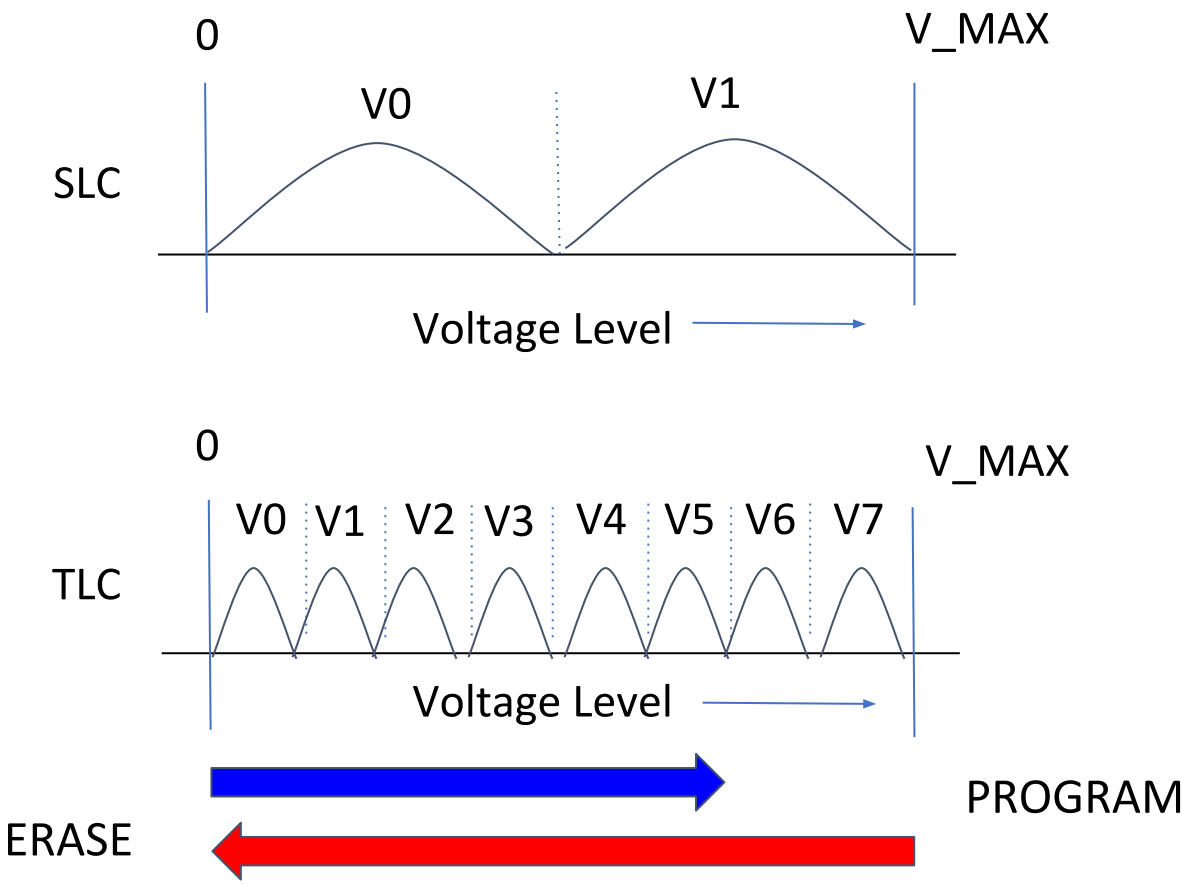
Rethinking WOM Codes to Enhance the Lifetime in new SSD Generations

Shehbaz Jaffer Kaveh Mahdaviani Bianca Schroeder

Computer Science
UNIVERSITY OF TORONTO

Future SSDs

Increased density – more bits per cell

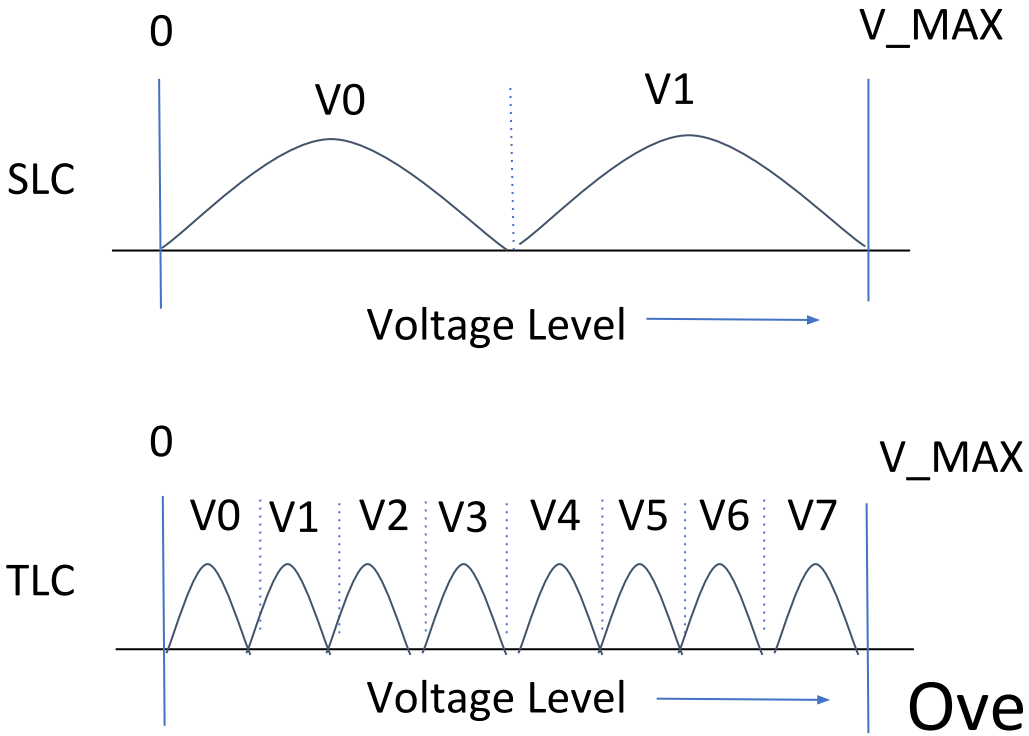


Voltage can only be increased (Program)

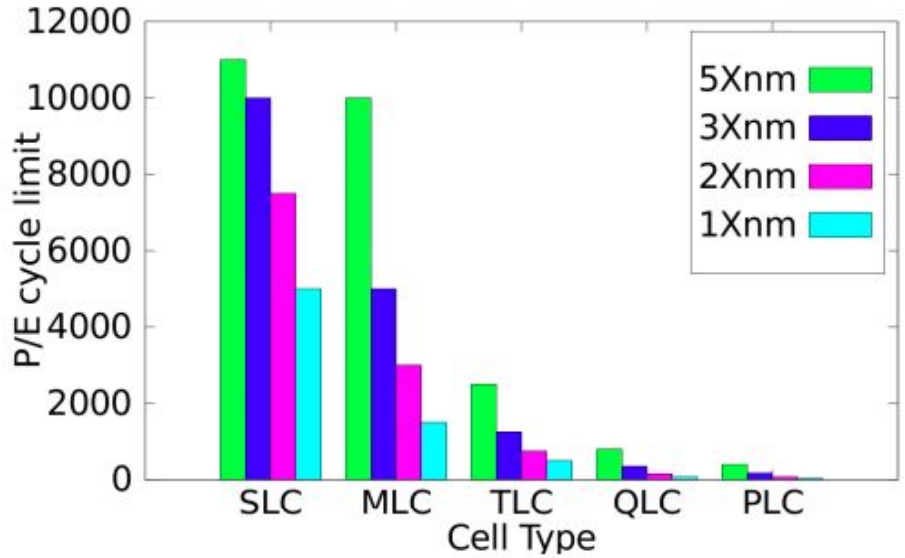
Voltage can be set to zero (Erase)

Future SSDs

Increased density – more bits per cell



Reduced Program and Erase (P/E) cycles



Overwrite between Erase

Write Once Memory Code

Bit-Based WOM Codes

Assumption: Bit values change from 0 to 1

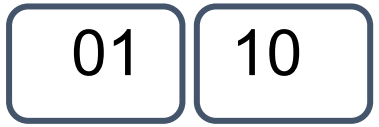
Data Word K = 2

Code word N=3

Data	Generation_1	Generation_2
00	000	111
01	100	011
10	010	101
11	001	110

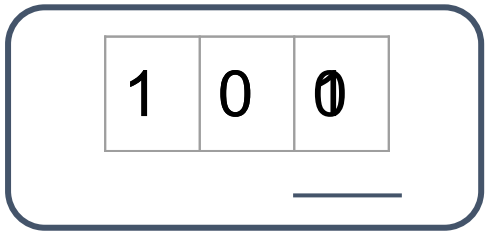
WOM (2, 3)

Data



4 bits

Media



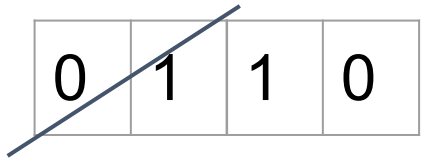
3 bits

NO_WOM

Data

01 10

Media



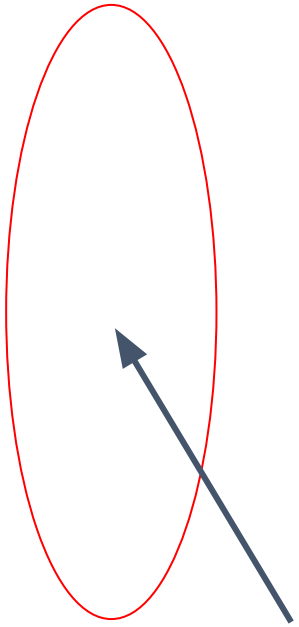
33 % Additional Data Before Erase

Problem

Bit constraint Affects Scalability as Flash gets denser

data	Gen_1	Gen_2	Gen_3
00	0000	1000	1111
01	0100	1100	1011
10	0010	1010	1101
11	0001	1001	1110

WOM (2, 4)

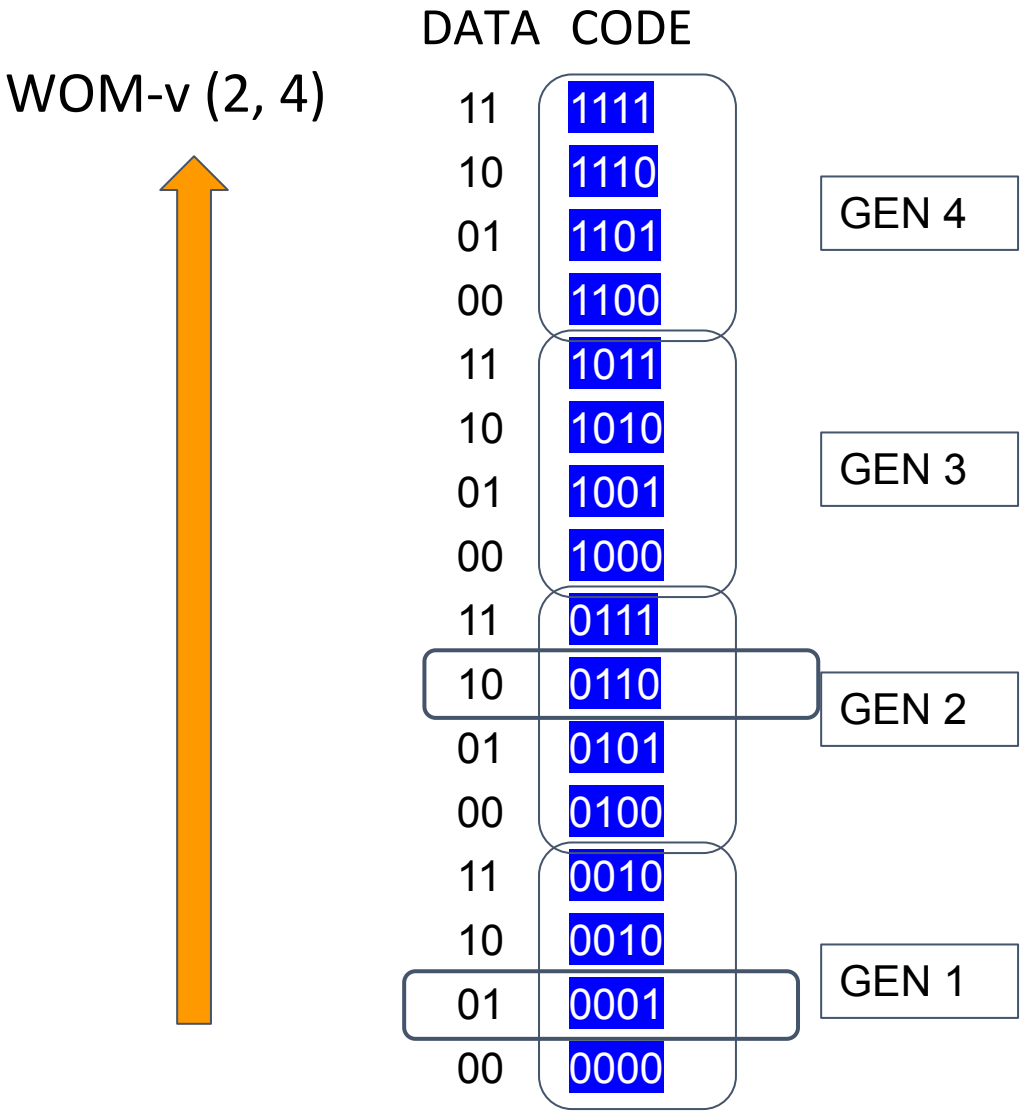


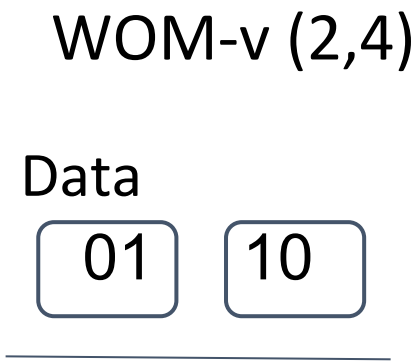
GEN 4 Not Possible!

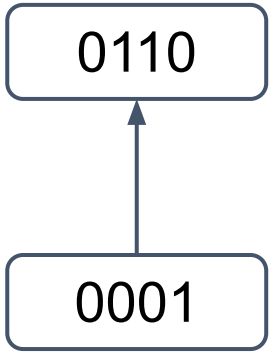
Only 50 % Additional Writes Possible Before Erase

More Gains Are Possible!

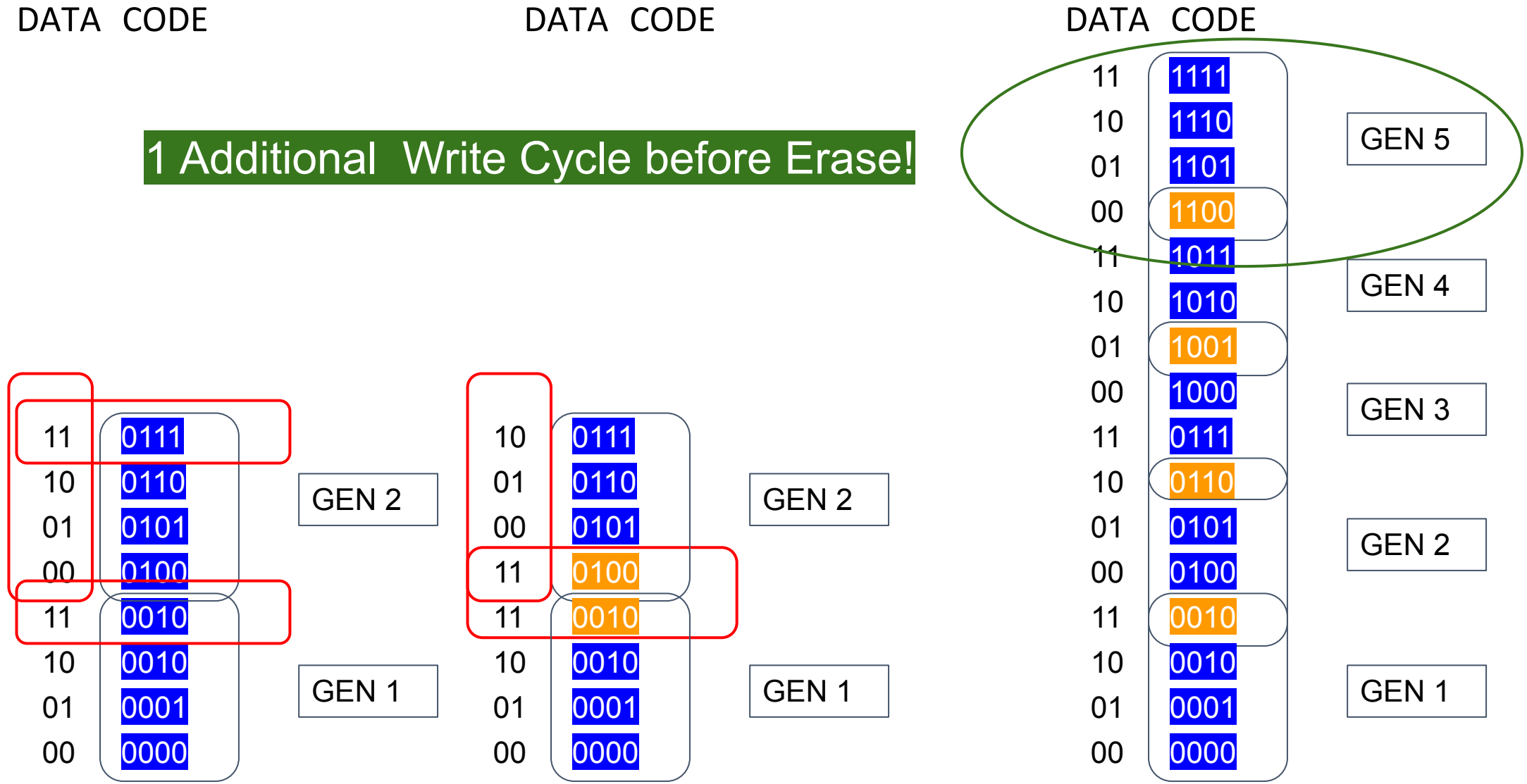
Our Solution: Voltage Based (WOM-v) Codes



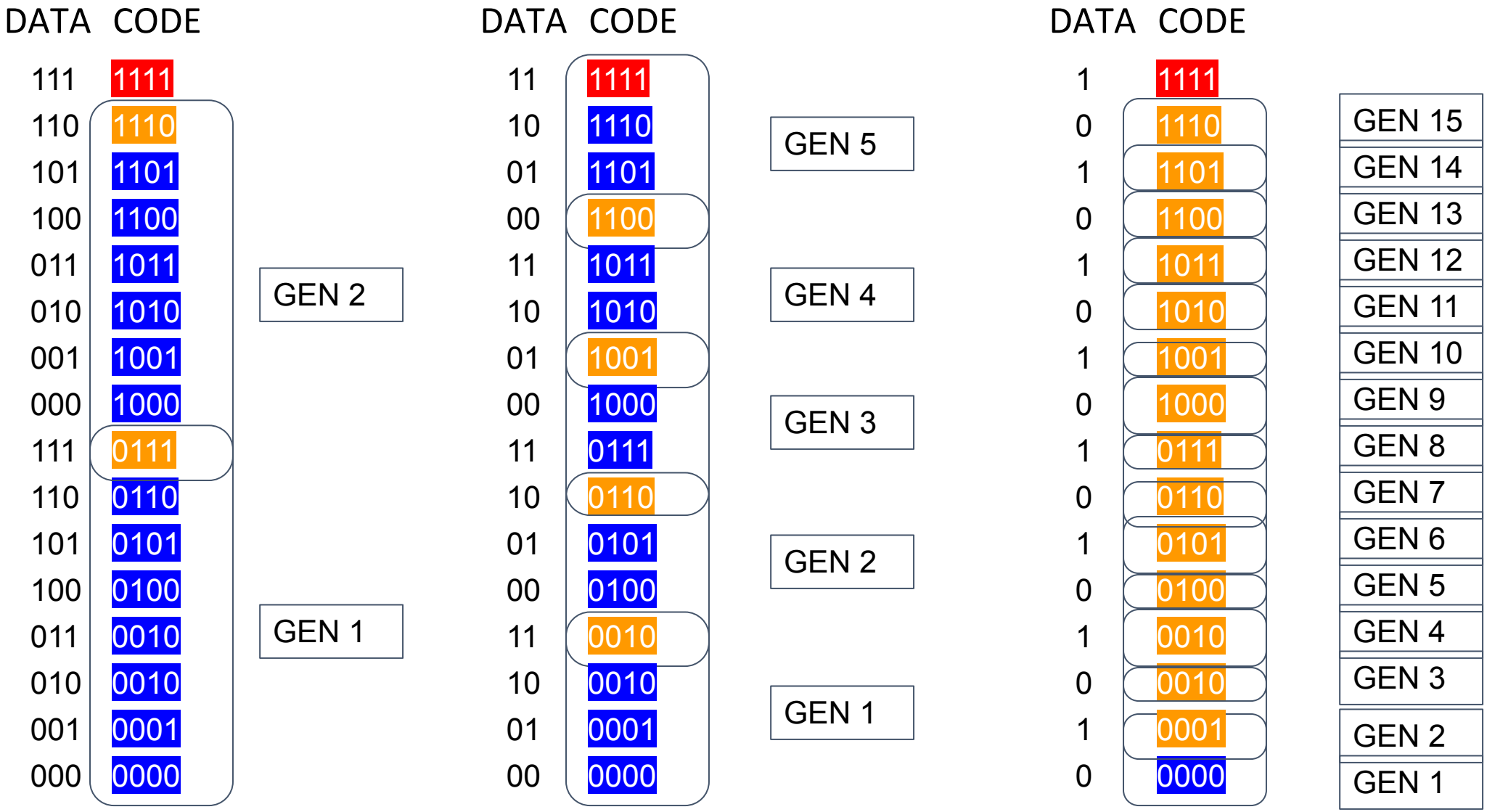




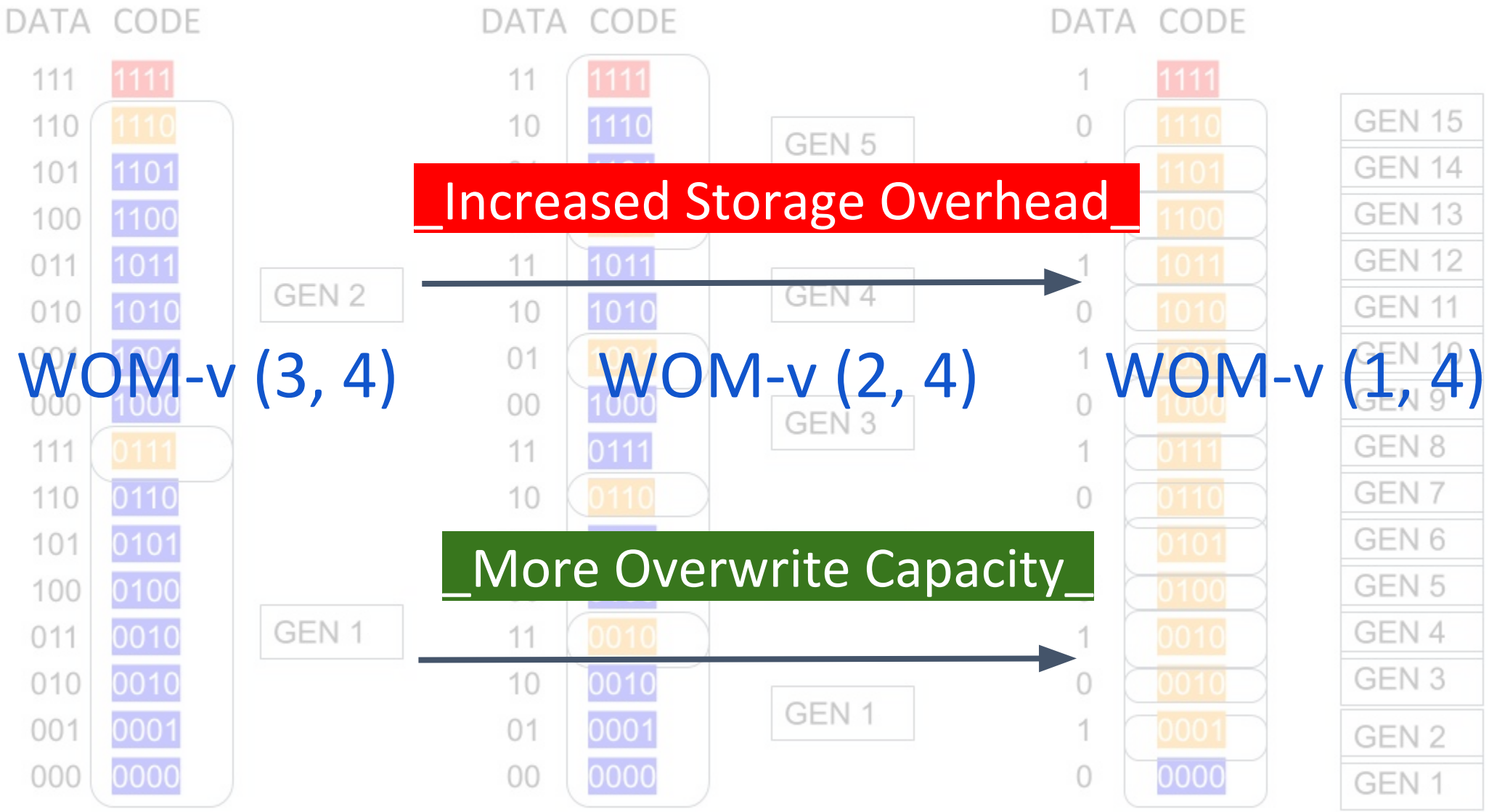
Optimization (I) - Code Word Sharing



Family of WOM-v Codes



Family of WOM-v Codes

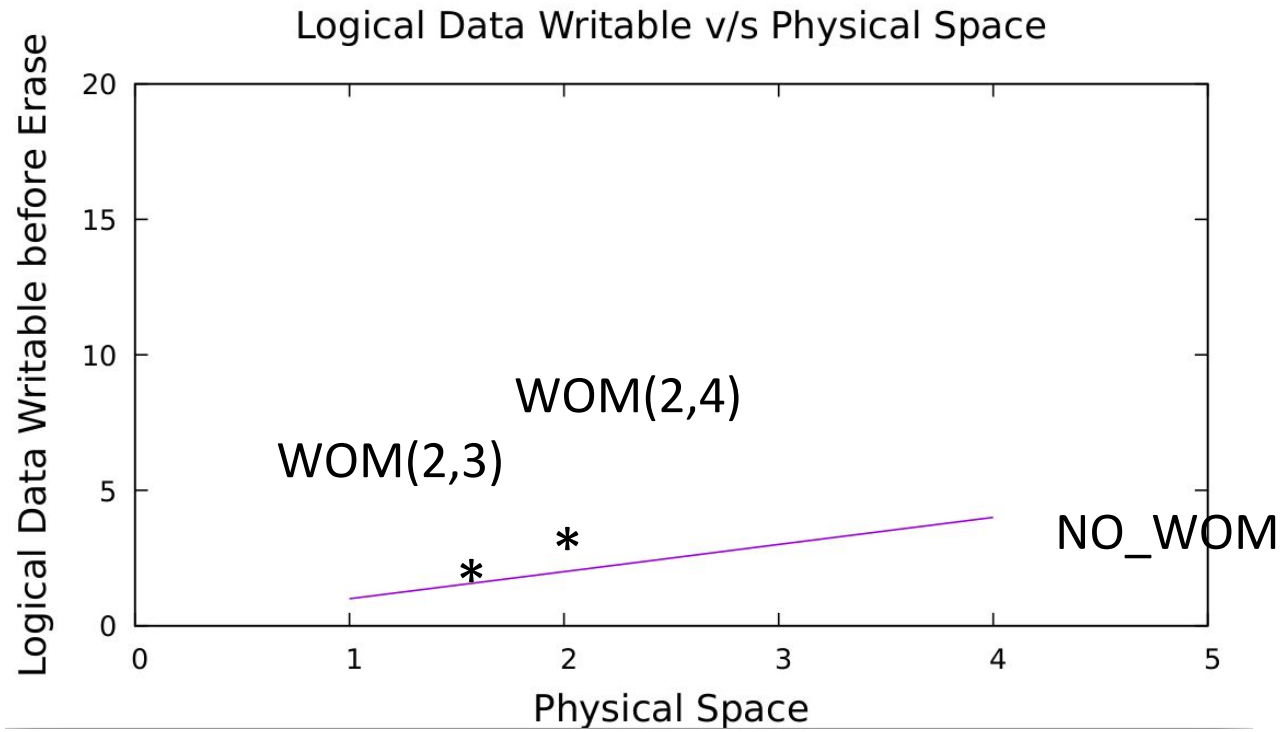


Increased Storage Overhead

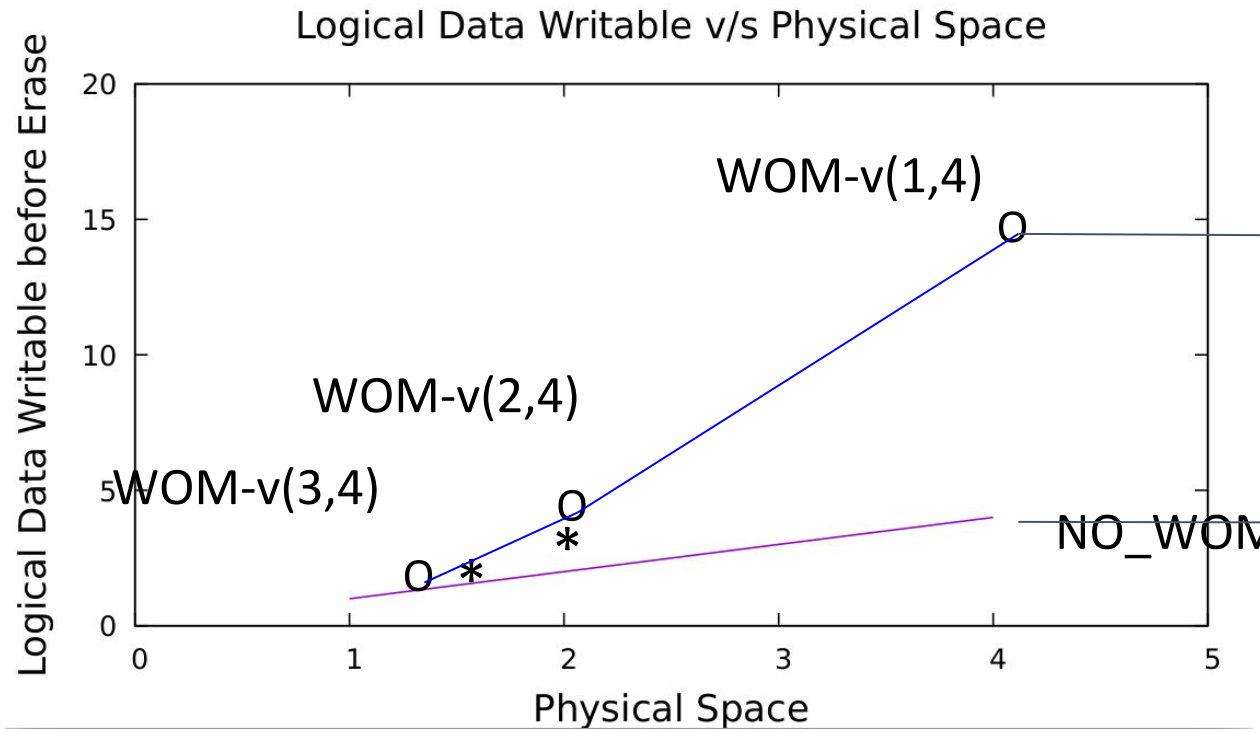
More Overwrite Capacity

WOM-v (3, 4) WOM-v (2, 4) WOM-v (1, 4)

Logical Data writable v/s Physical Space



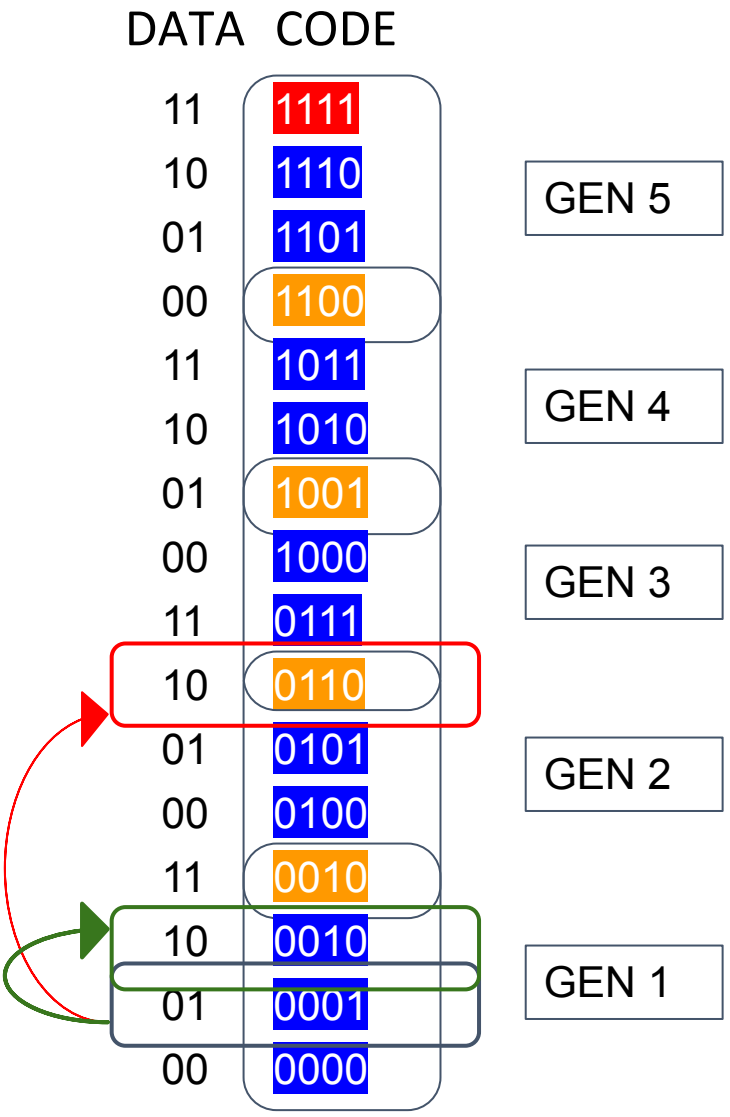
Logical Data writable v/s Physical Space



375 % More Writes

Tune WOM-v Code based on Physical Storage Capacity and Overwrites Required before Erase.

Optimization (II) Same Generation Transition

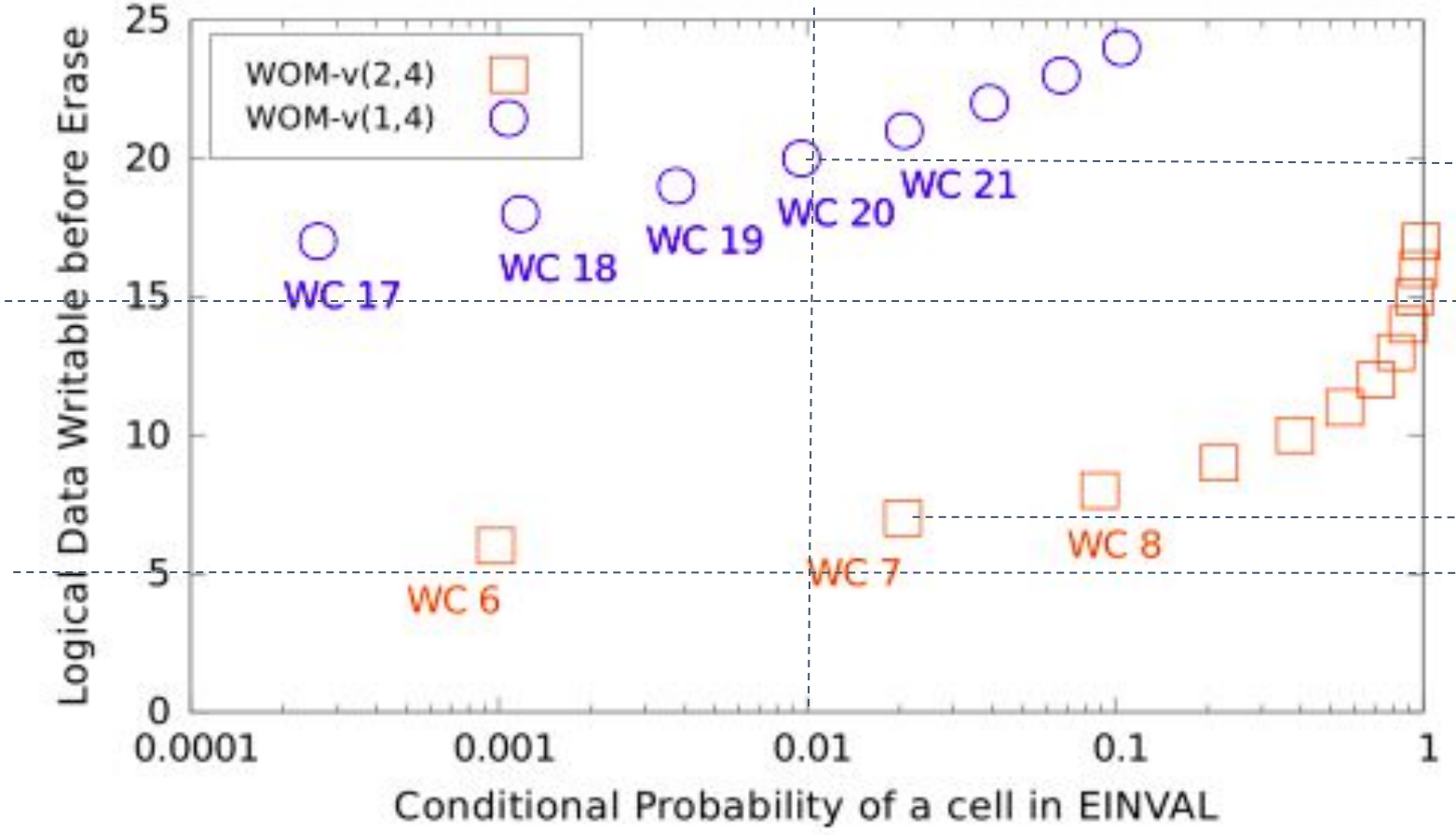


Objective – reach V_MAX as slow as possible

WOM-v (2,4)

Data	01	10
Code	0110	0010
	↑	↑
Code	0001	0001

Cell in V_MAX after Write Cycles

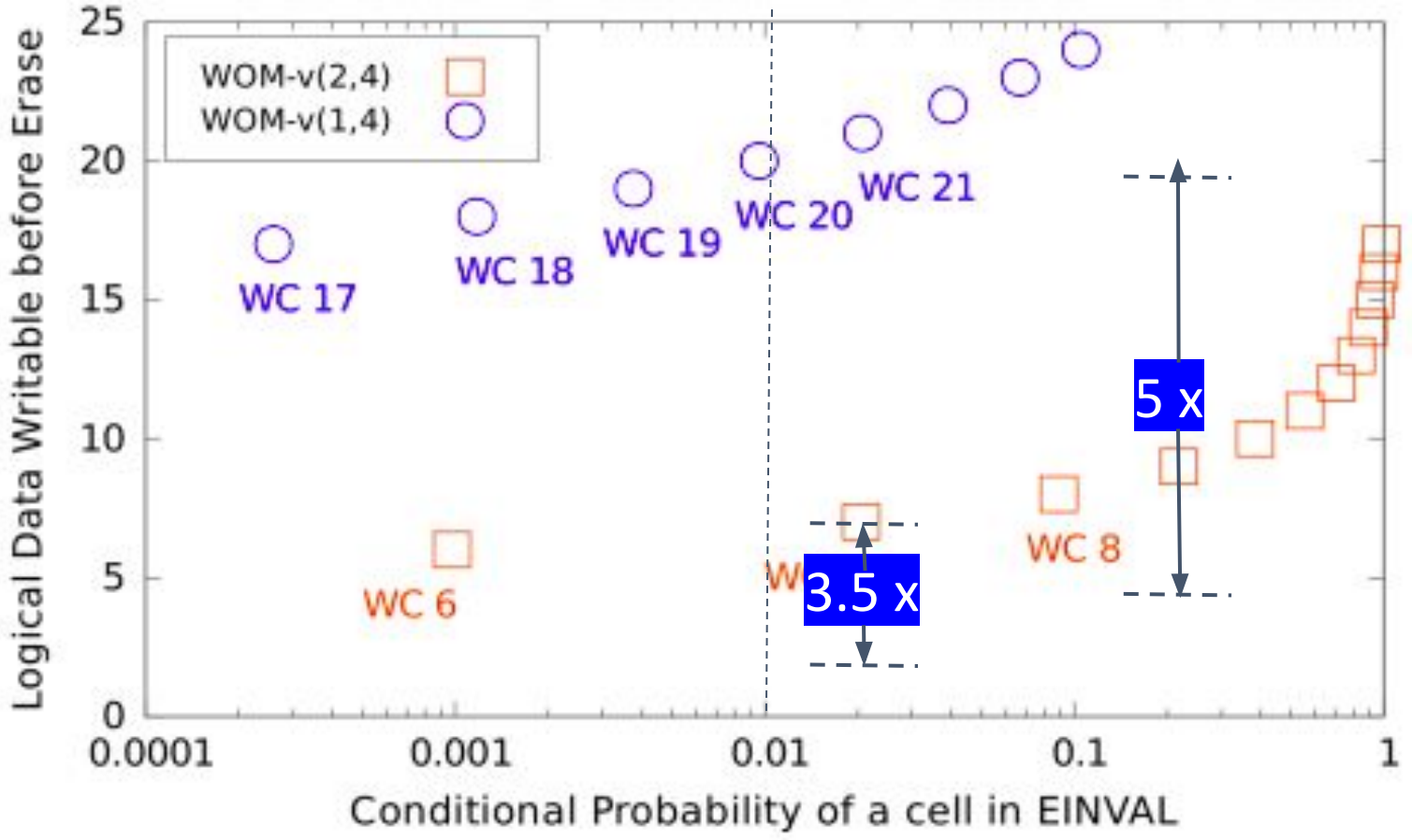


WOM-v (1,4)
Additional WC

WOM-v (2,4)
Additional WC

Many cells remain underutilized

Cell in V_MAX after Write Cycles



Many cells remain underutilized

Conclusion

- Novel Family of WOM Coding scheme for future Solid State Drives.
- Efficient Easy to implement – simple table lookups
- Generic - can be adopted to any N-Level Cell Drive.
- Extendable beyond theoretical writes with minor overheads.

Increase Logical Write Before Erase up to 500% for QLC Drives!

Thank you

Shehbaz Jaffer Kaveh Mahdaviani Bianca Schroeder

{shehbaz,mahdaviani,bianca}@cs.toronto.edu

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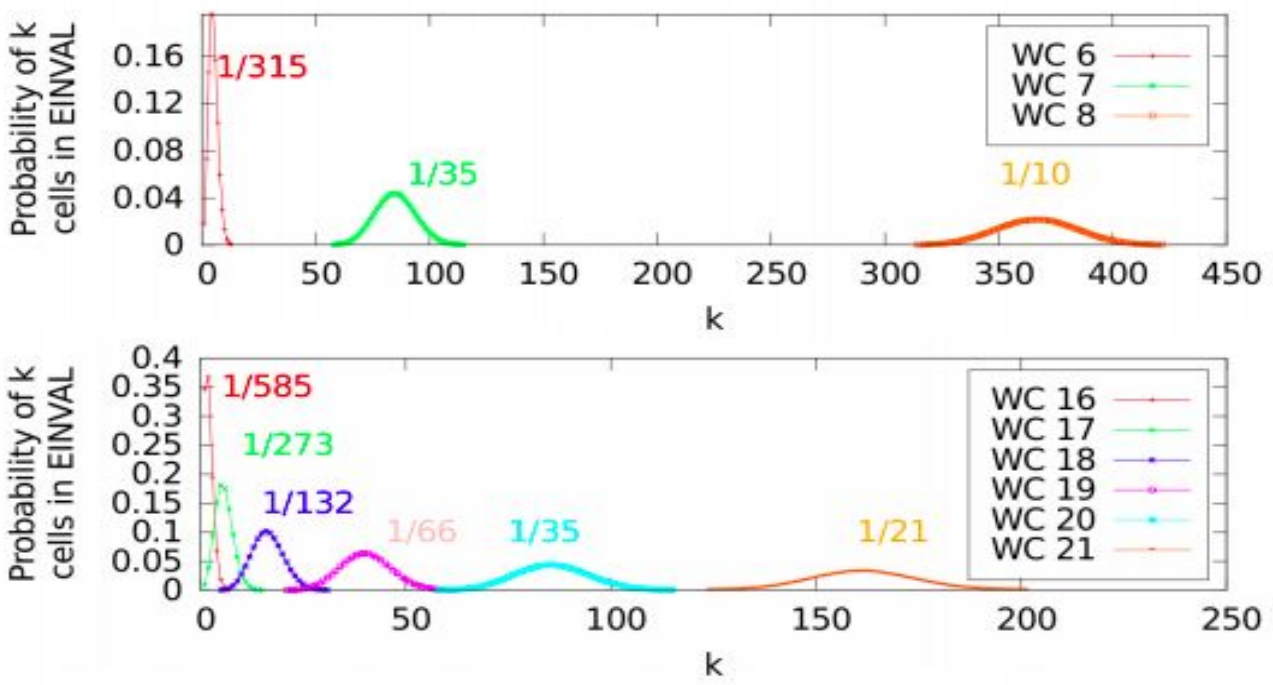
Discussion

- Using Over-provisioned Space v/s ECC
- Existing QLC RBER Rates.
- Voltage Transition Limitations.
- Effects of Re-programming on flash lifetime
- Impact on simplifying SSD circuit design

Backup Slides

ECC Design criteria



Binomial distribution for reaching EINVAL
Page Size = 4096
1/p denotes 1 additional ECC correction bits that needs to be maintained for every p data bits to continue reprogramming underutilized cells WC times.

Need more write Cycles?
Add More Redundancy.

Upto 500% Additional Data Can be Written Before Erase!