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Errata Slip #2

In the paper "Exploring the Design Space of Page Management for Multi-Tiered Memory Systems" by Jonghyeon Kim, Wonkyo Choe, and Jeongseob Ahn, *Ajou University* (Friday session, "My Tail Never Has Any Latency: OS & Hardware," pp. 715–728 of the Proceedings), the authors have provided the following correction.

Original figure:

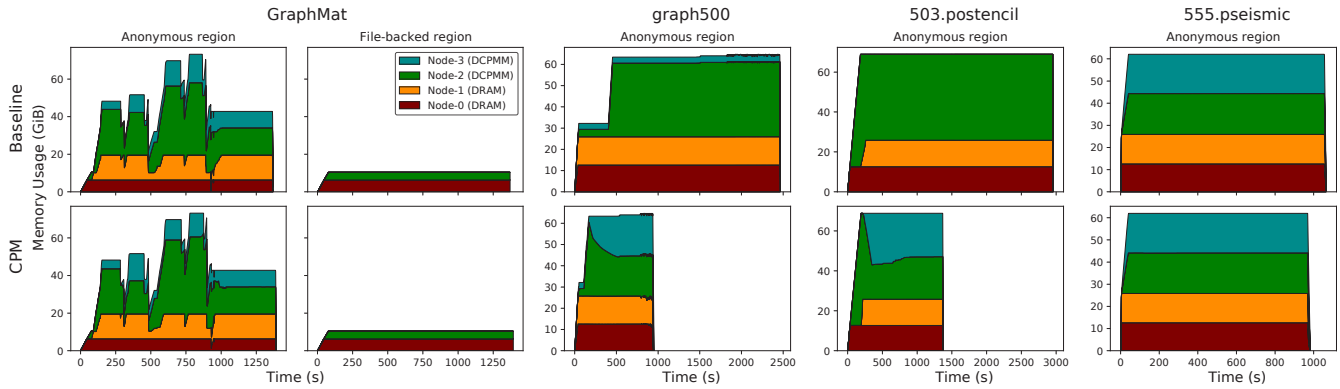

Figure 10: Memory usage across DRAM and DCPMM nodes (Baseline vs. CPM)

Corrected figure:

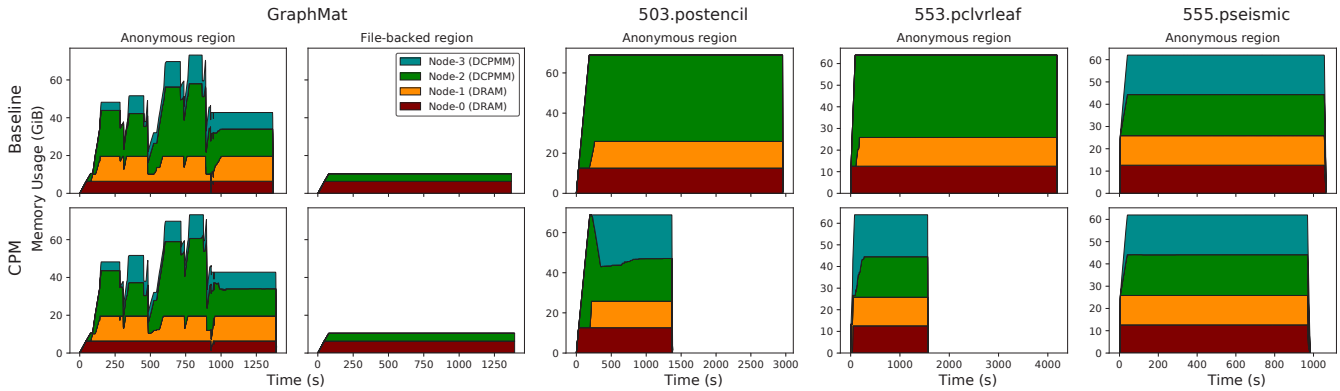

Figure 10: Memory usage across DRAM and DCPMM nodes (Baseline vs. CPM)

Explanation:

In the original version, Figure 10 is incorrect for graph500 because the result is from our scheme OPM, not CPM. To make Figure 10 consistent with the explanation in Section 5.2 (Distribution of memory usage), we replace graph500 with 553.pclvrleaf.