How Sharp is SHARP?

WOOT'19@USENIX-SECURITY

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Chavhan Sujeet Yashavant *(Indian Institute of Technology Kanpur),*
Biswabandan Panda *(Indian Institute of Technology Kanpur), and*
Vishal Gupta *(Manipal University Jaipur and Indian Institute of Technology Kanpur)*

SHARP [Yan et al., ISCA ‘17]

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Secure hierarchy-aware cache replacement policy

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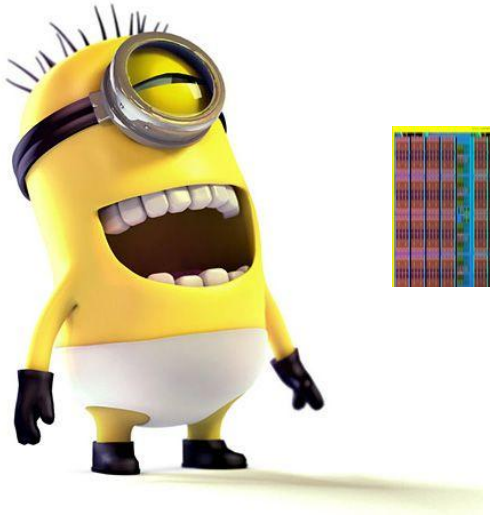
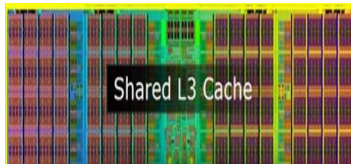
Secure hierarchy-aware cache replacement policy

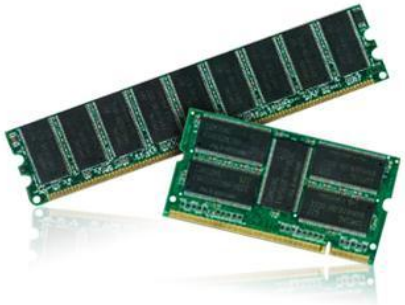
Mitigation for side-channel attacks

Side Channel Attacks

Attacker

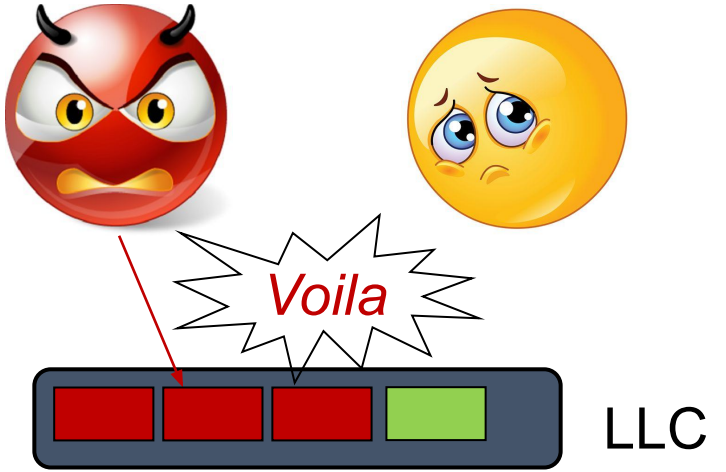






Victim

Eviction based Cache Attacks: (Prime+Probe)



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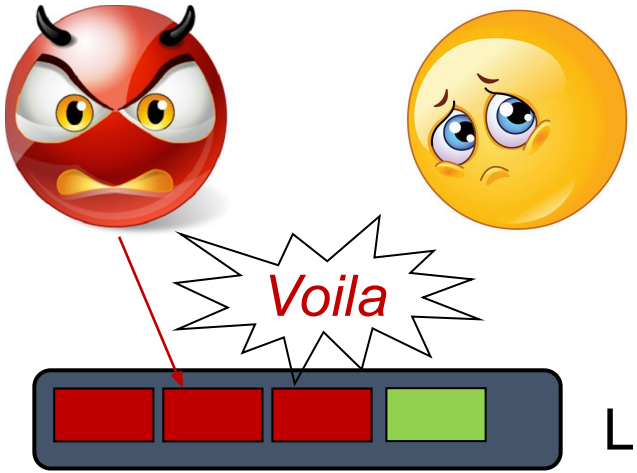
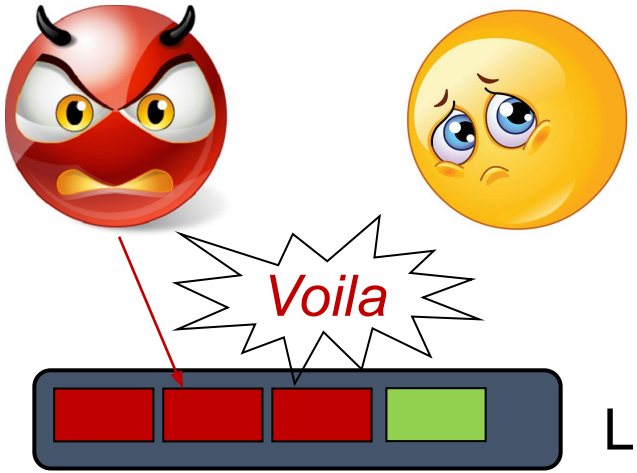


Step 0: Attacker *fills* the entire shared cache (set)

Eviction based Cache Attacks: (Prime+Probe)



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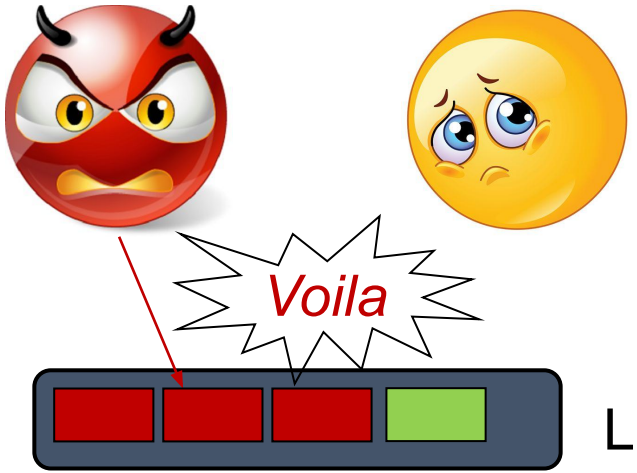

Step 0: Attacker *fills* the entire shared cache (set)

Step 1: Victim *evicts* cache blocks while running

Step 2: Attacker *probes* the cache set

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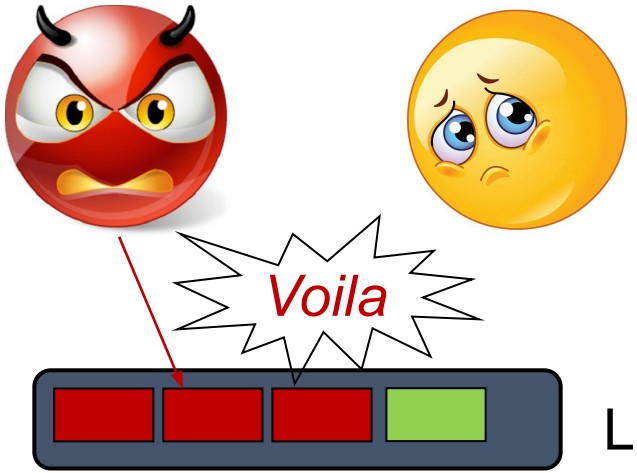

Step 0: Attacker *fills* the entire shared cache (set)

Step 1: Victim *evicts* cache blocks while running

Step 2: Attacker *probes* the cache set

If *misses* then victim has accessed the set

Various Mitigations

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Cache Layout [HPCA ‘16]

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Cache Layout [HPCA ‘16]

Fuzzing the timer [ISCA ‘12]

Various Mitigations

Cache Layout [HPCA ‘16]

Fuzzing the timer [ISCA ‘12]

Cache Addressing [MICRO ‘18]

Various Mitigations

Cache Layout [HPCA ‘16]

Fuzzing the timer [ISCA ‘12]

Cache Addressing [MICRO ‘18]

Cache replacement policy [ISCA ‘17]

SHARP [Yan et al., ISCA ‘17]

Secure hierarchy-aware cache replacement policy

Mitigation for side-channel attacks

SHARP [Yan et al., ISCA ‘17]

Secure hierarchy-aware cache replacement policy

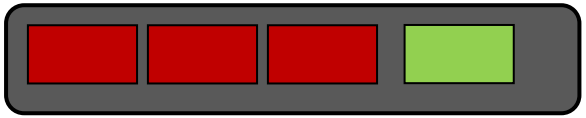
Mitigation for side-channel attacks

Prevents cross-core back invalidation

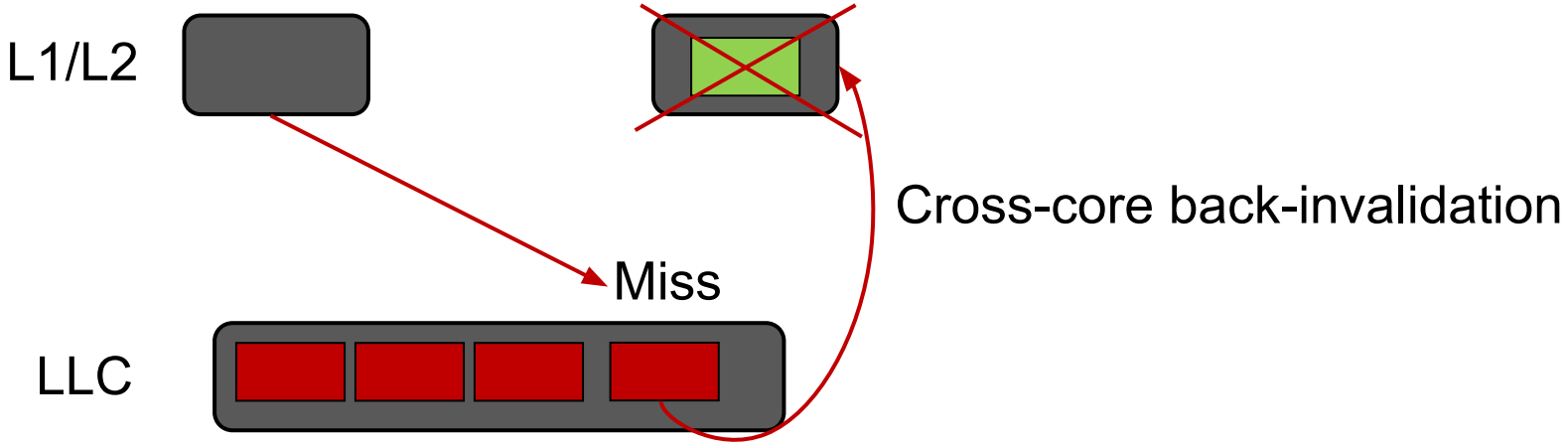
Cross-core Back-Invalidation - I

L1/L2

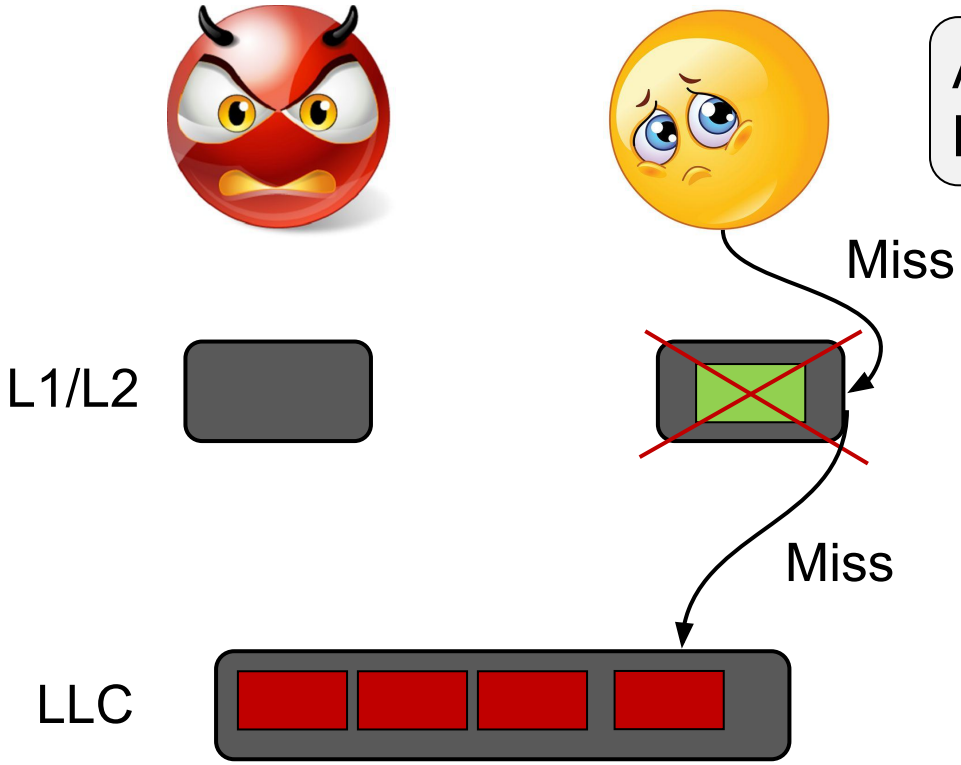
LLC



Cross-core Back-Invalidation - II



Cross-core Back-Invalidation - III



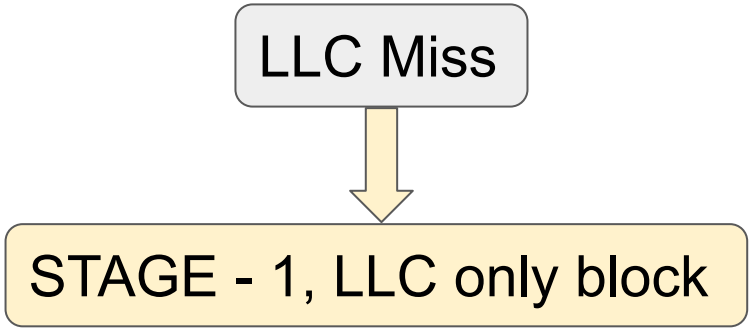
Attacker knows whether victim has accessed it or not

How SHARP Works?

How SHARP Works?

LLC Miss

How SHARP Works?



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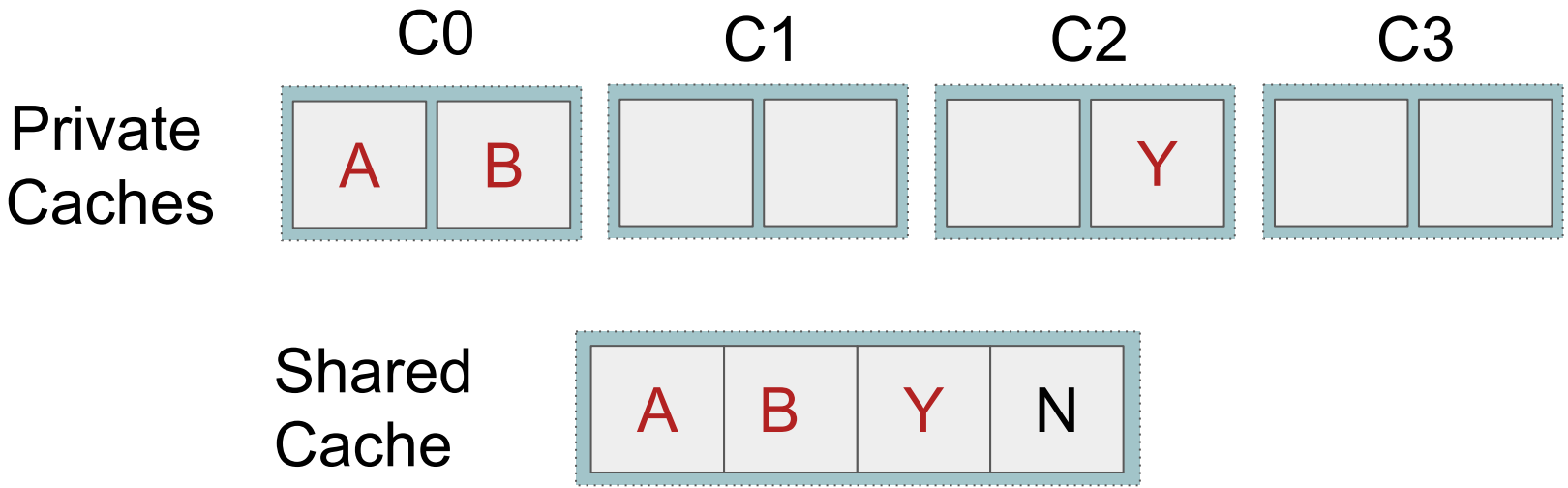
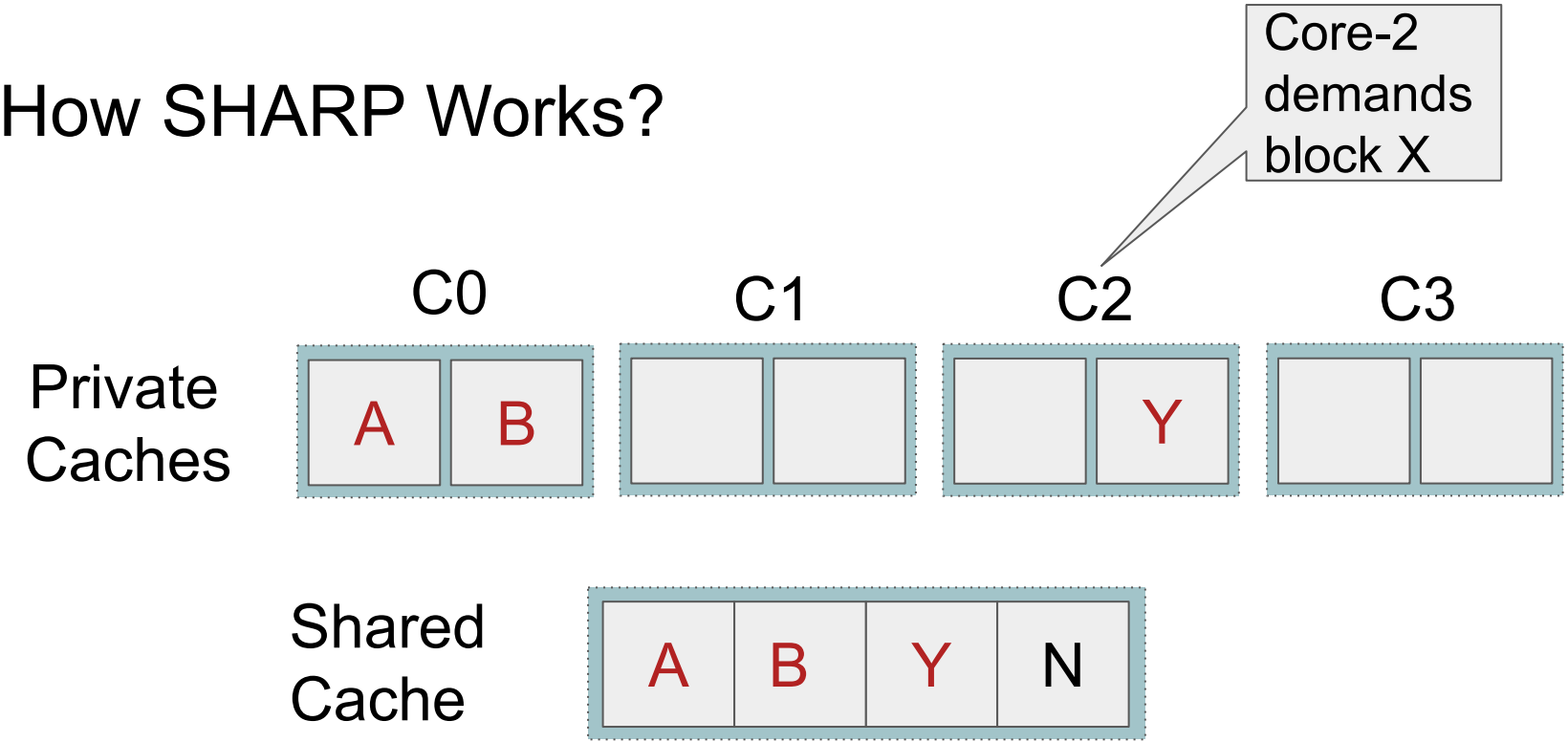


Stage-1

How SHARP Works?



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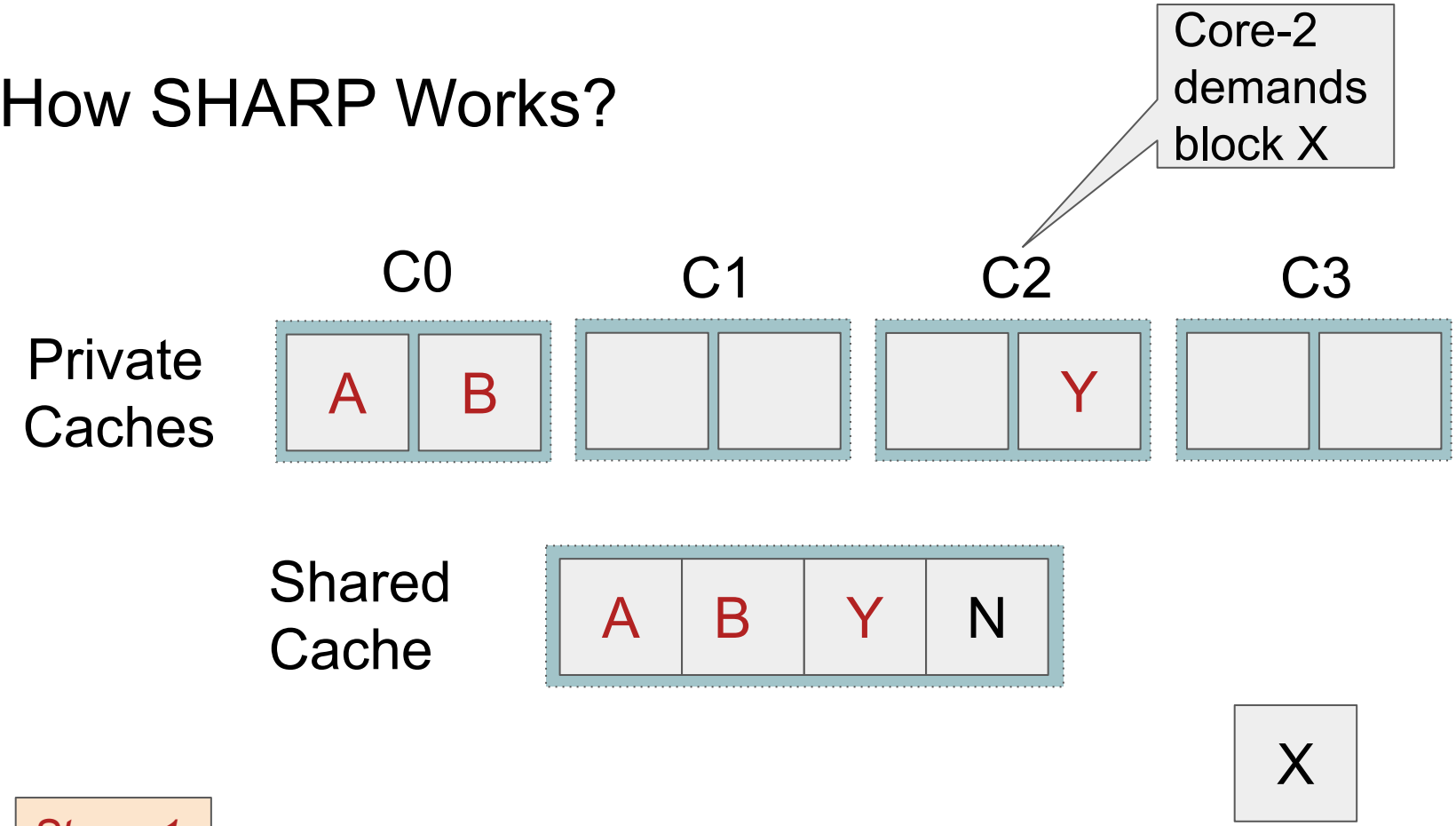

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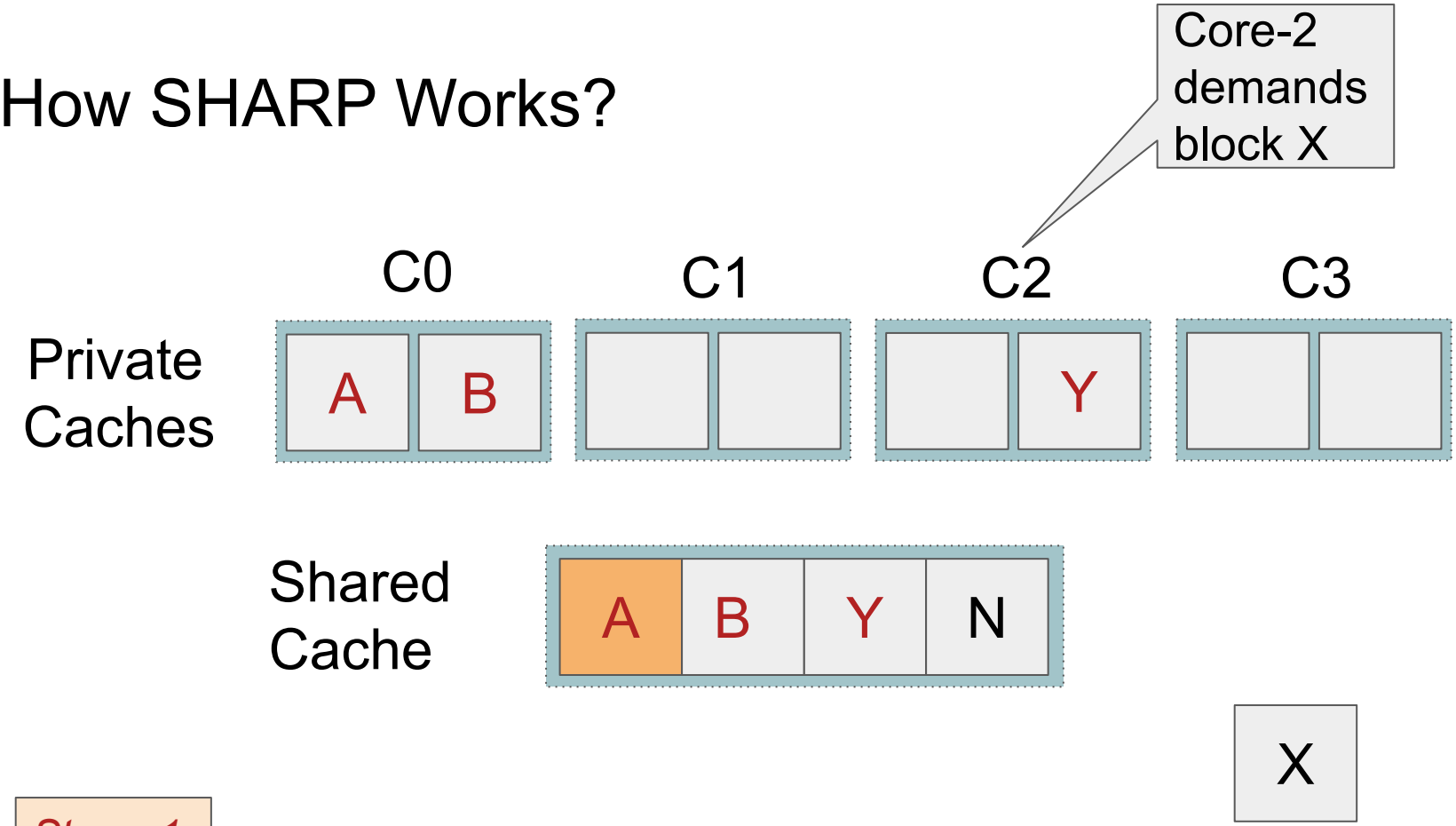

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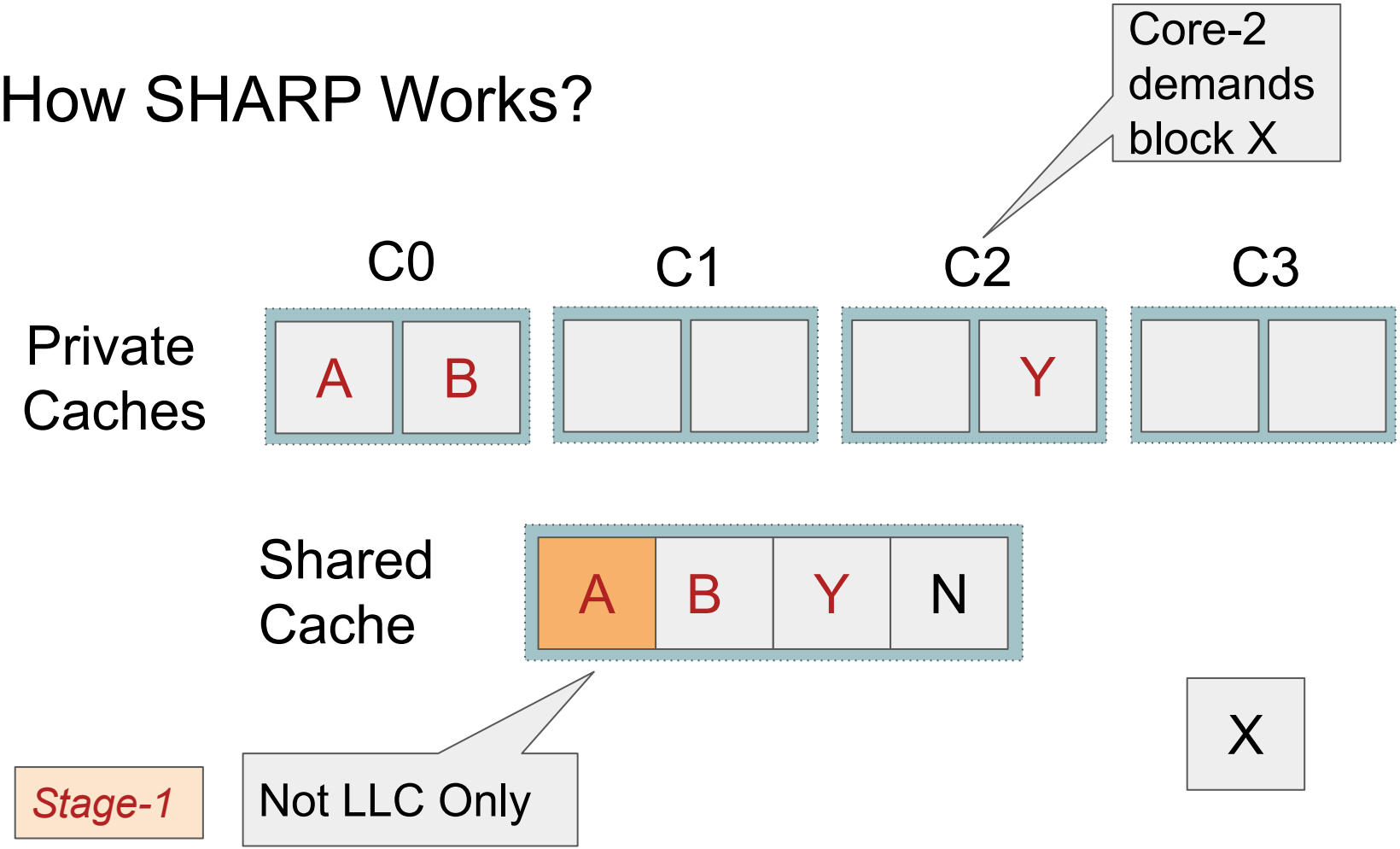

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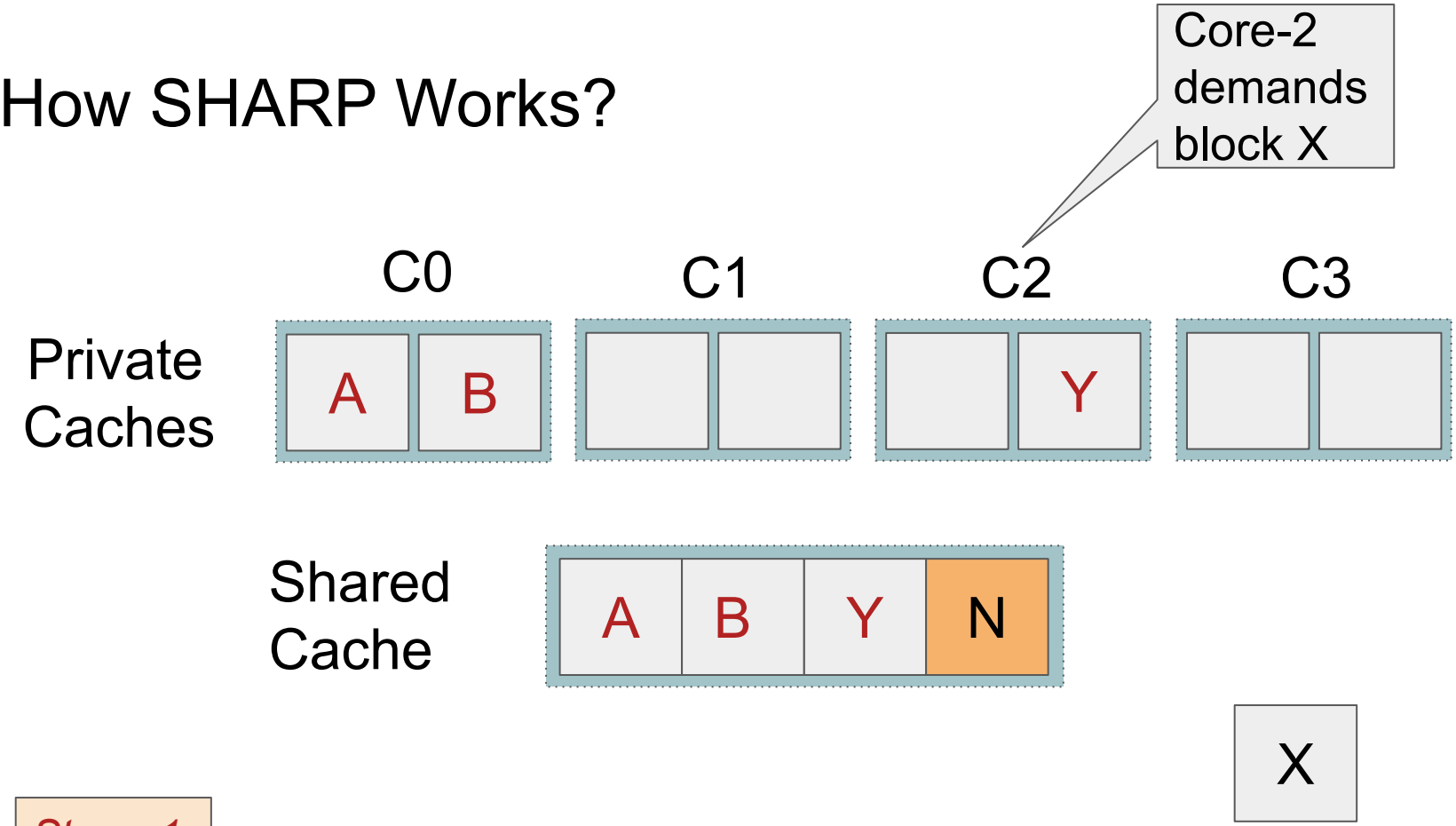

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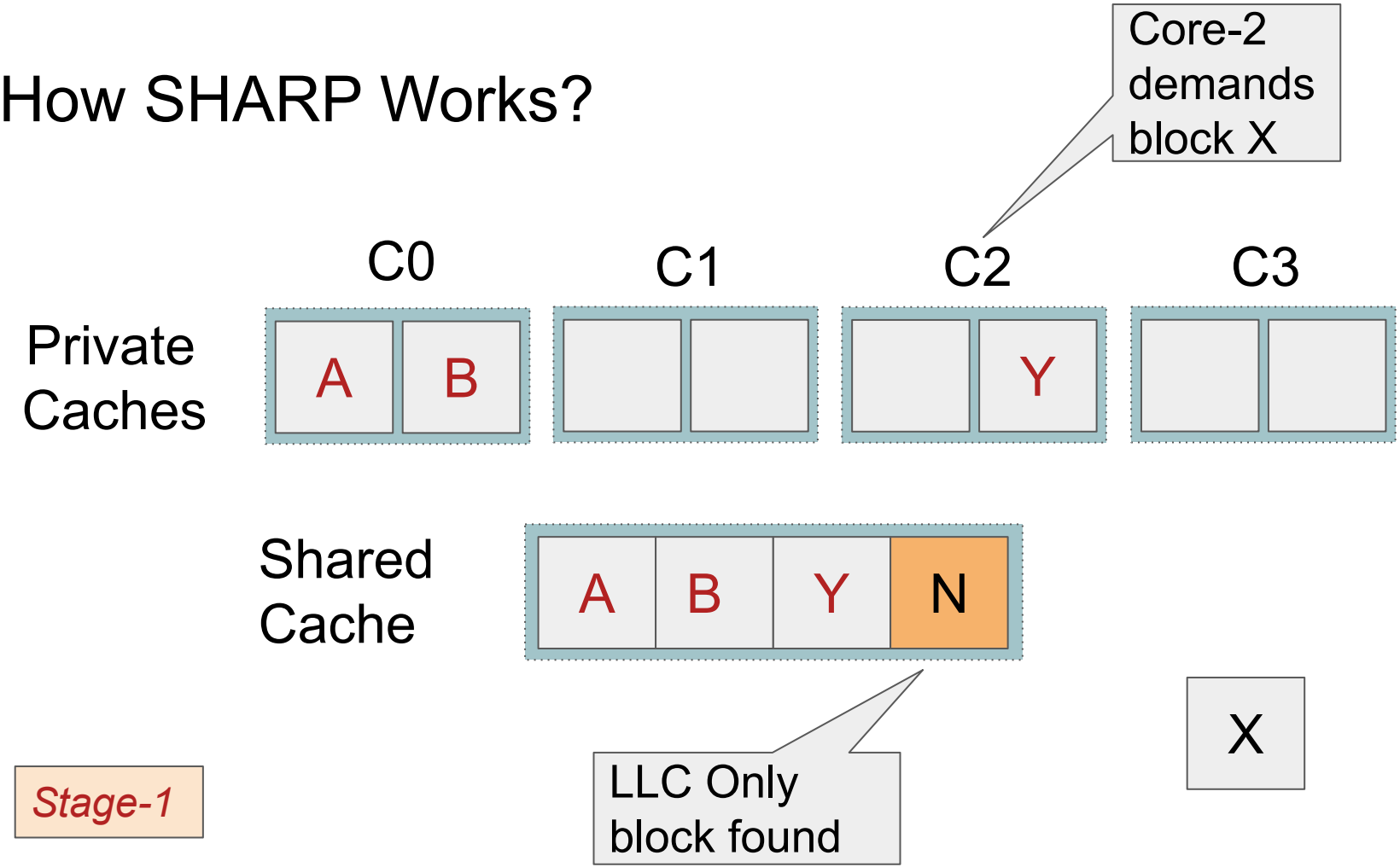

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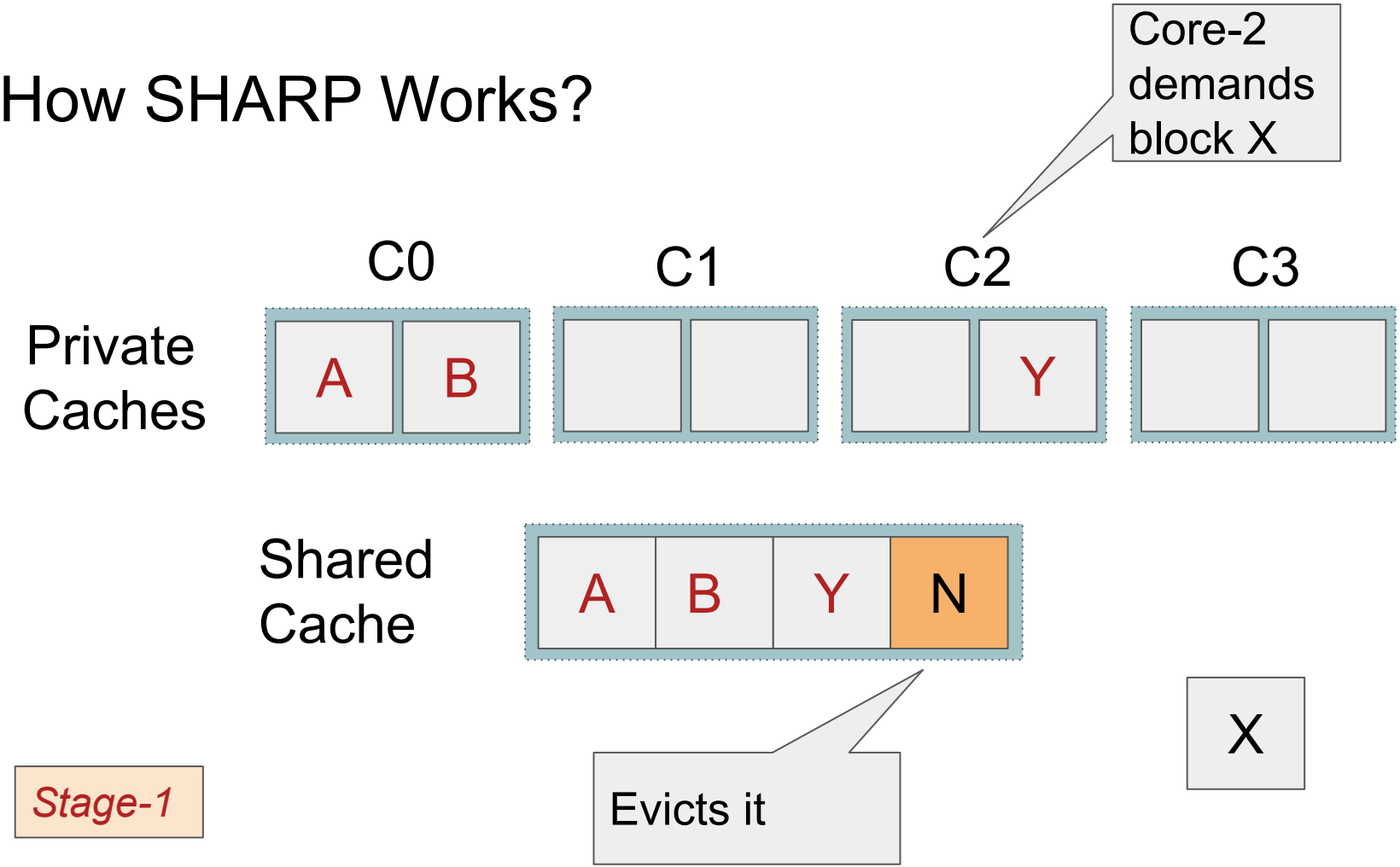

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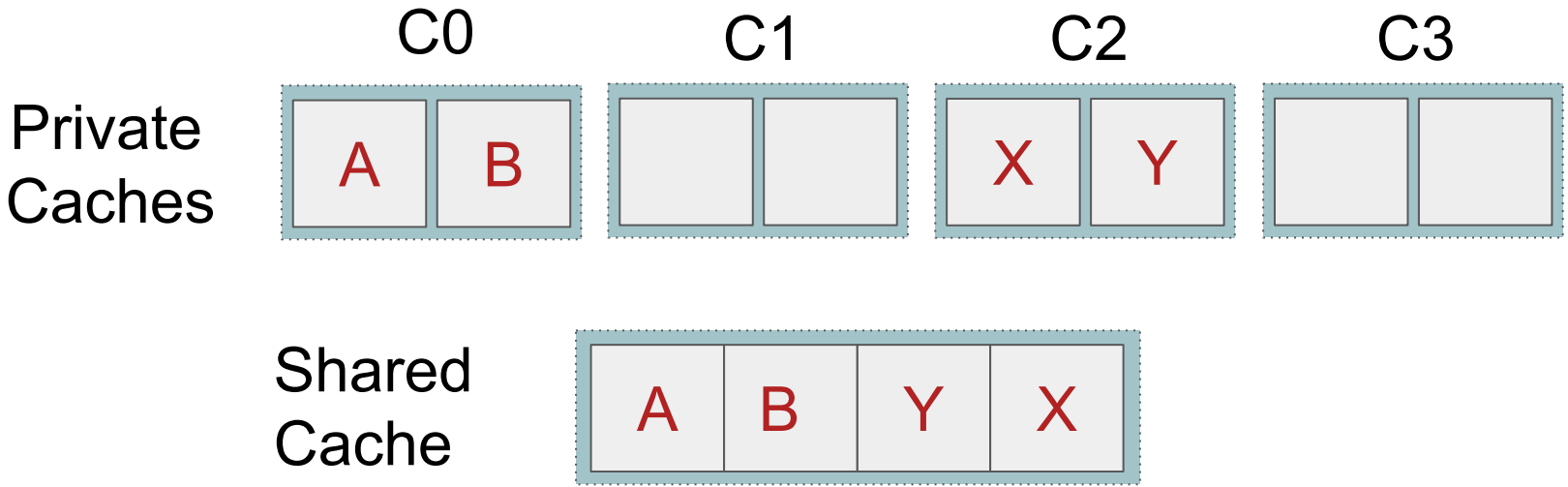

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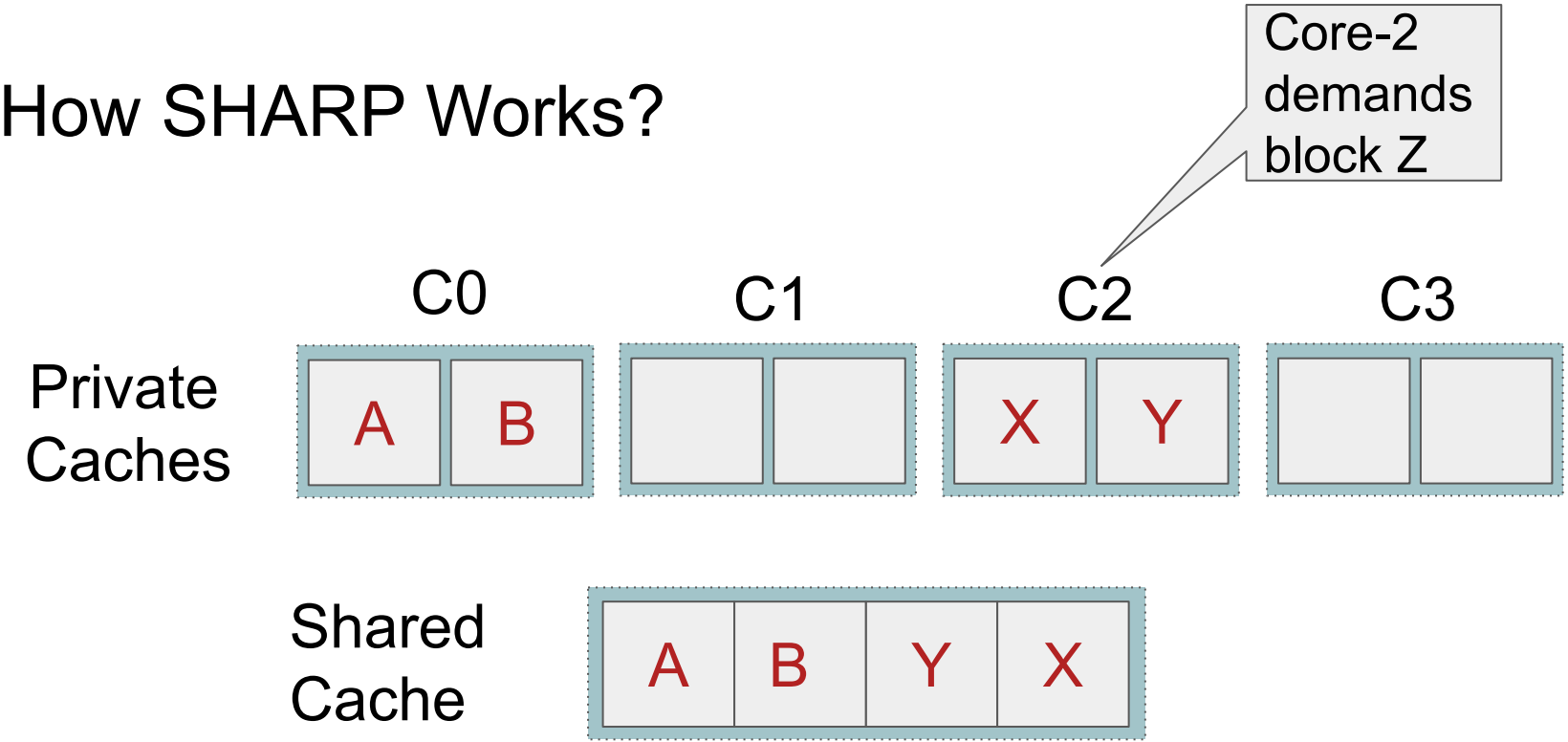

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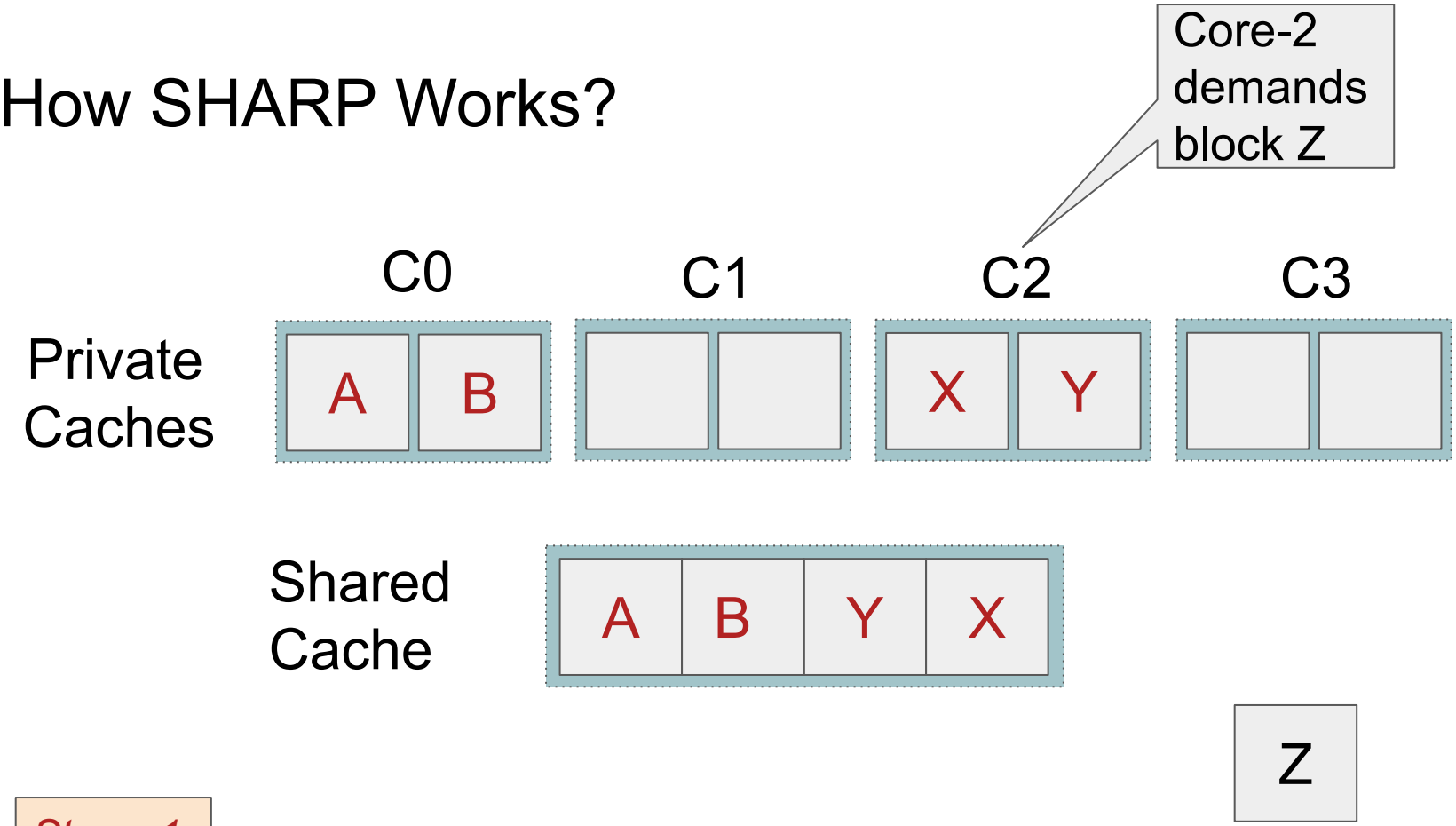

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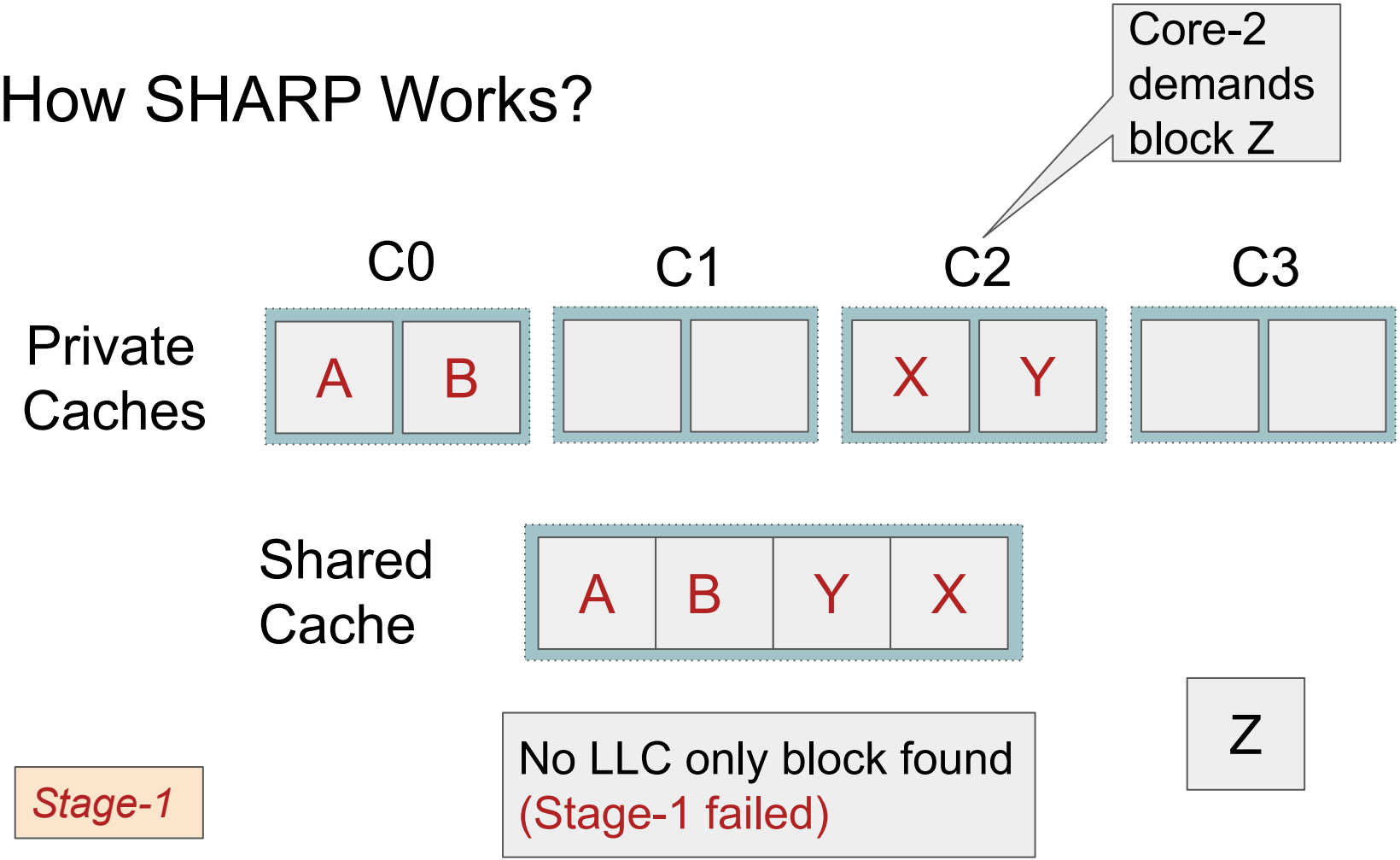

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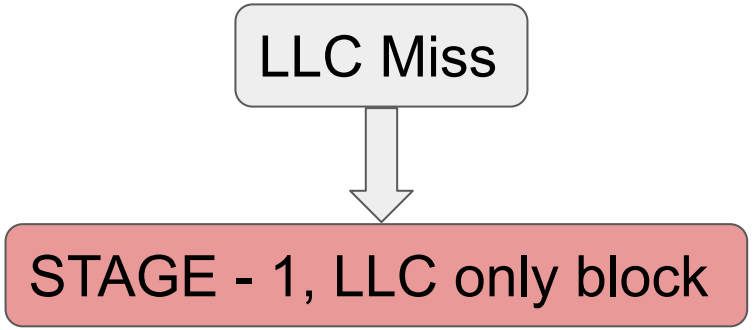

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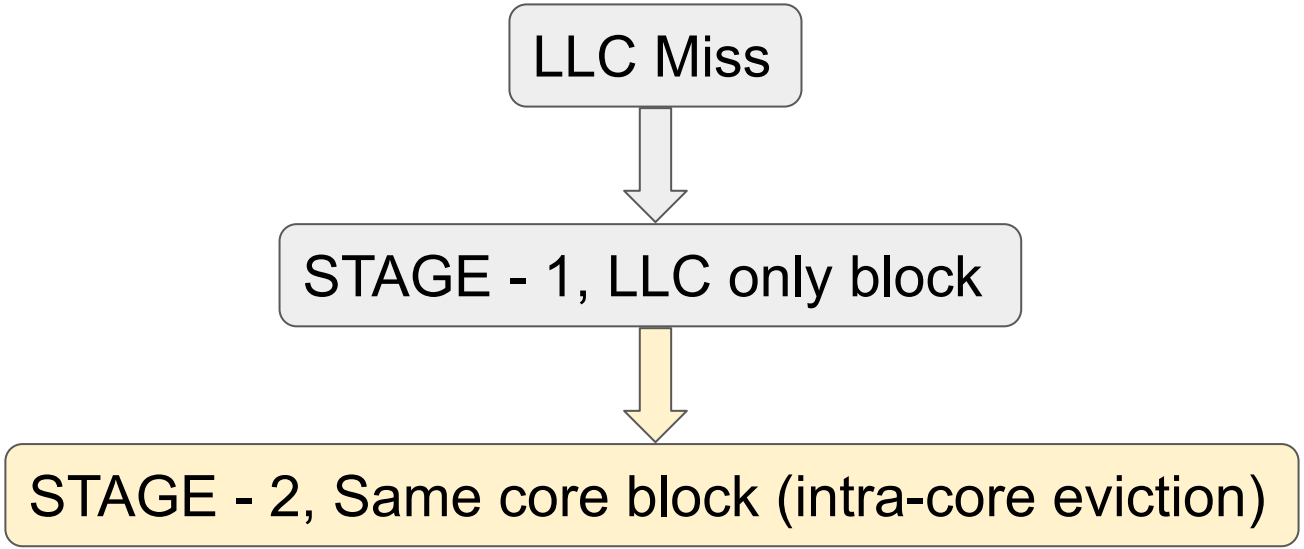

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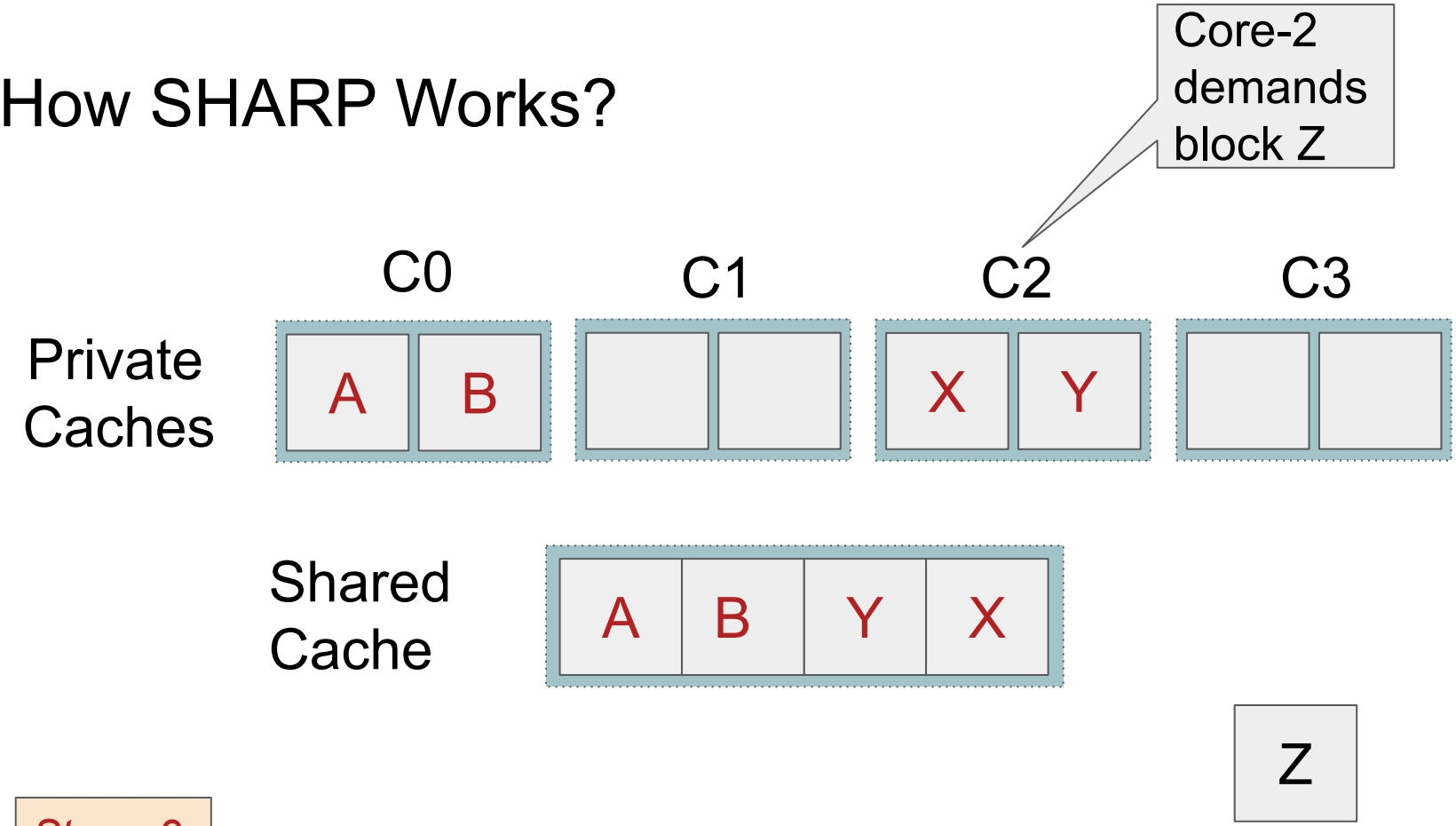

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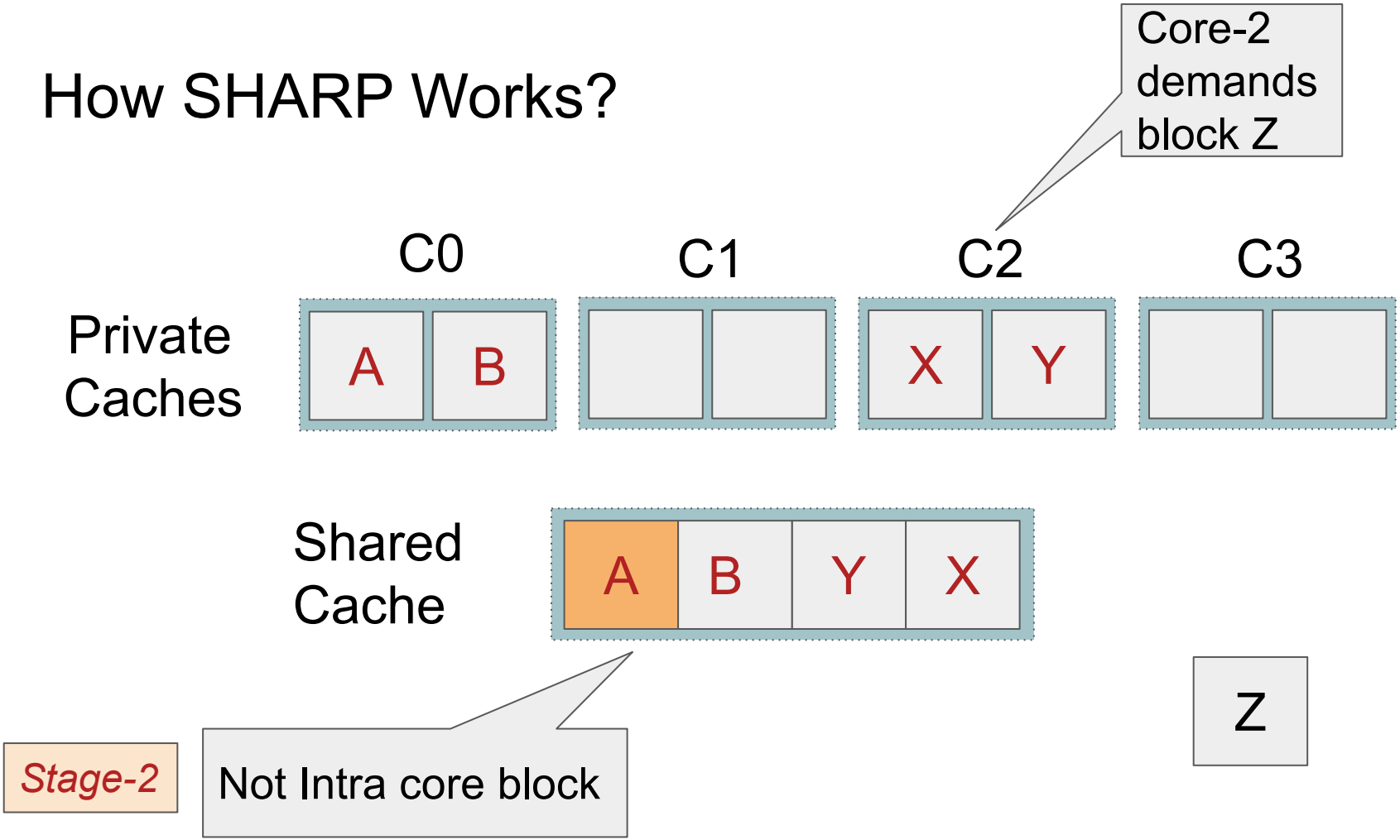

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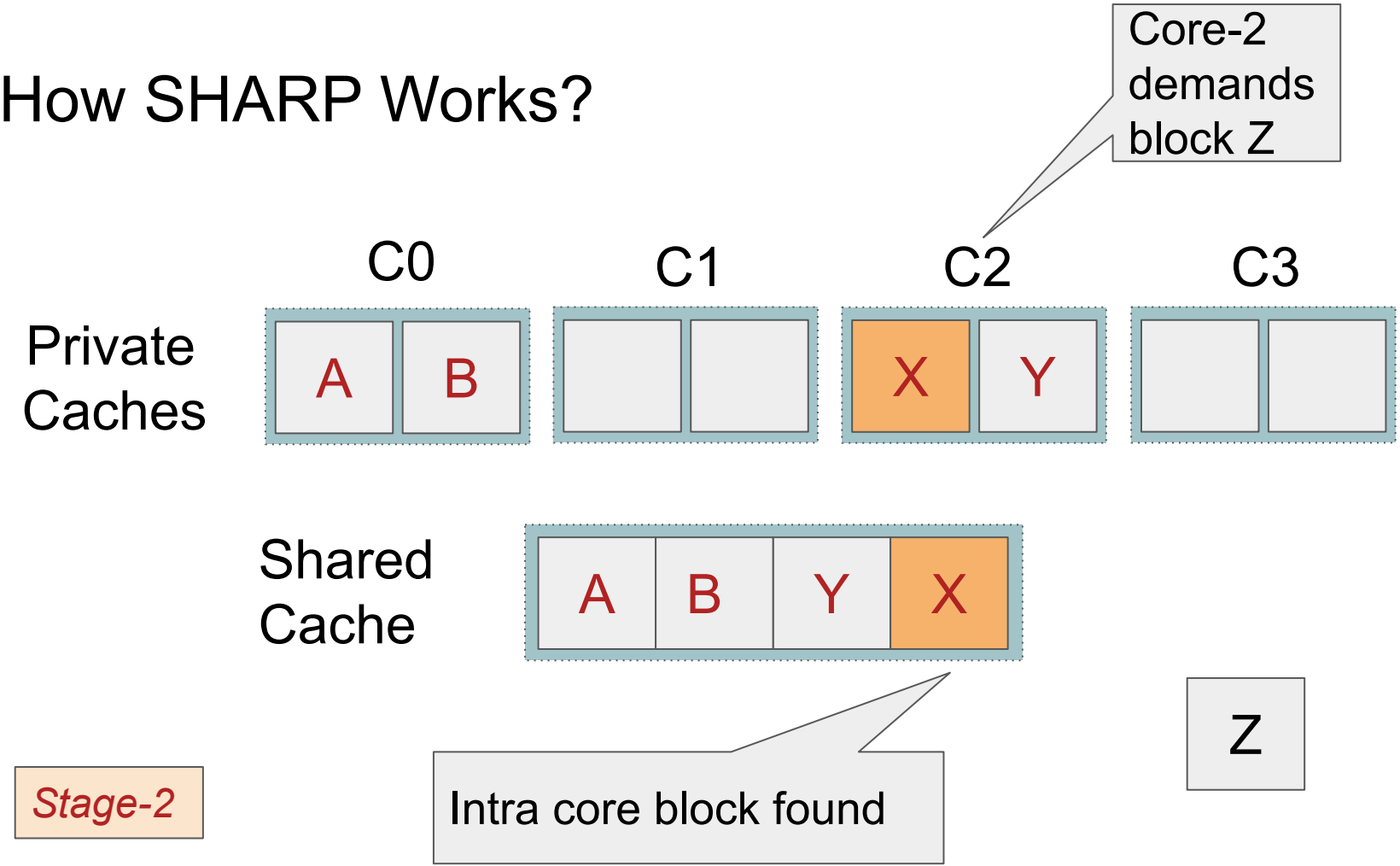

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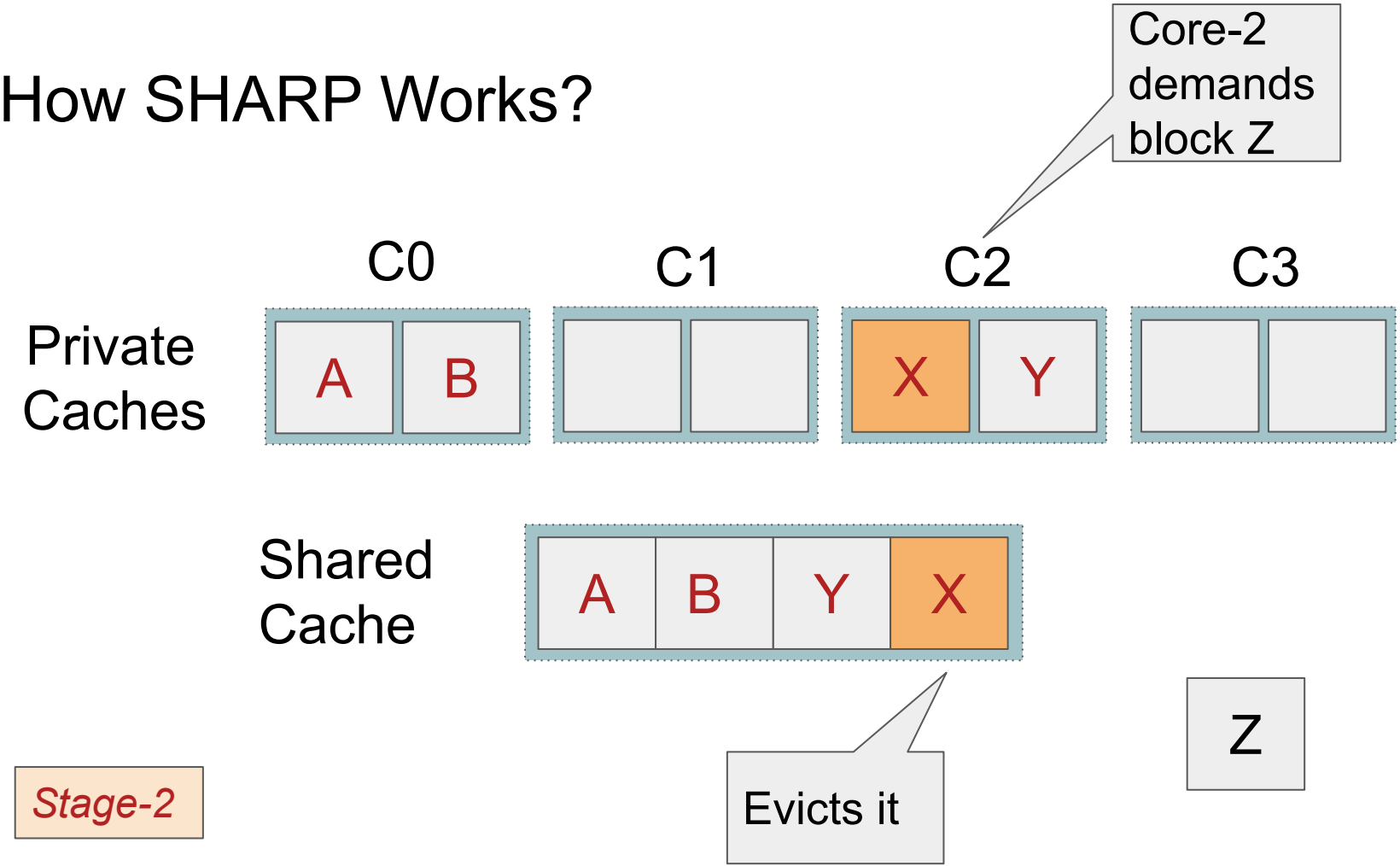

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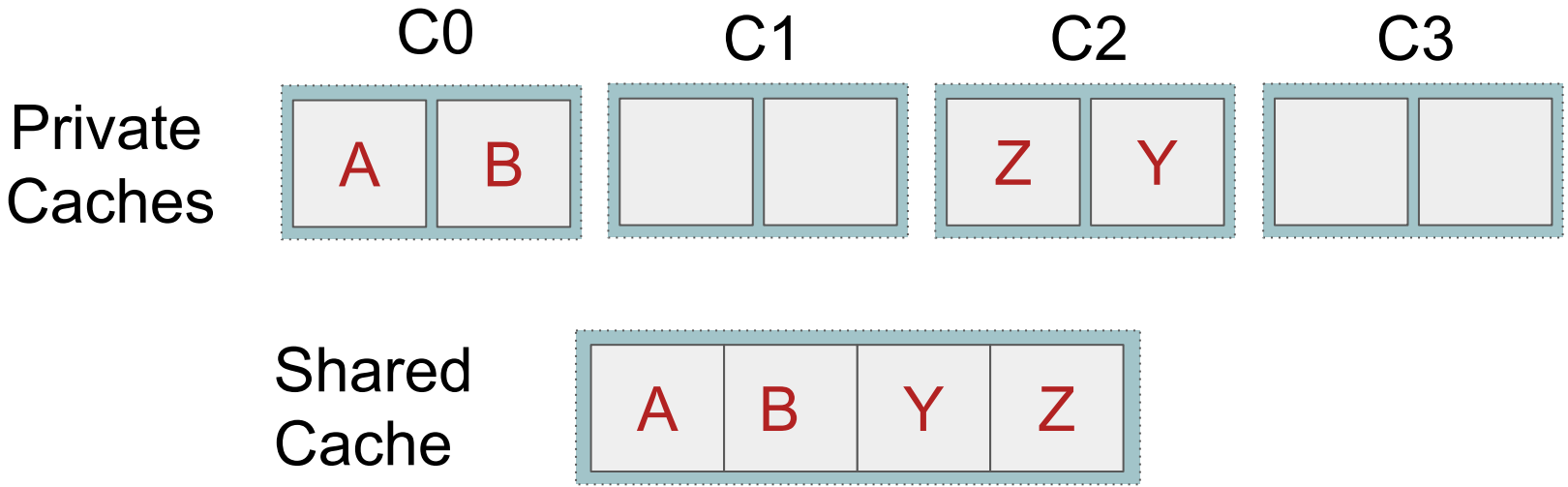

Stage-2

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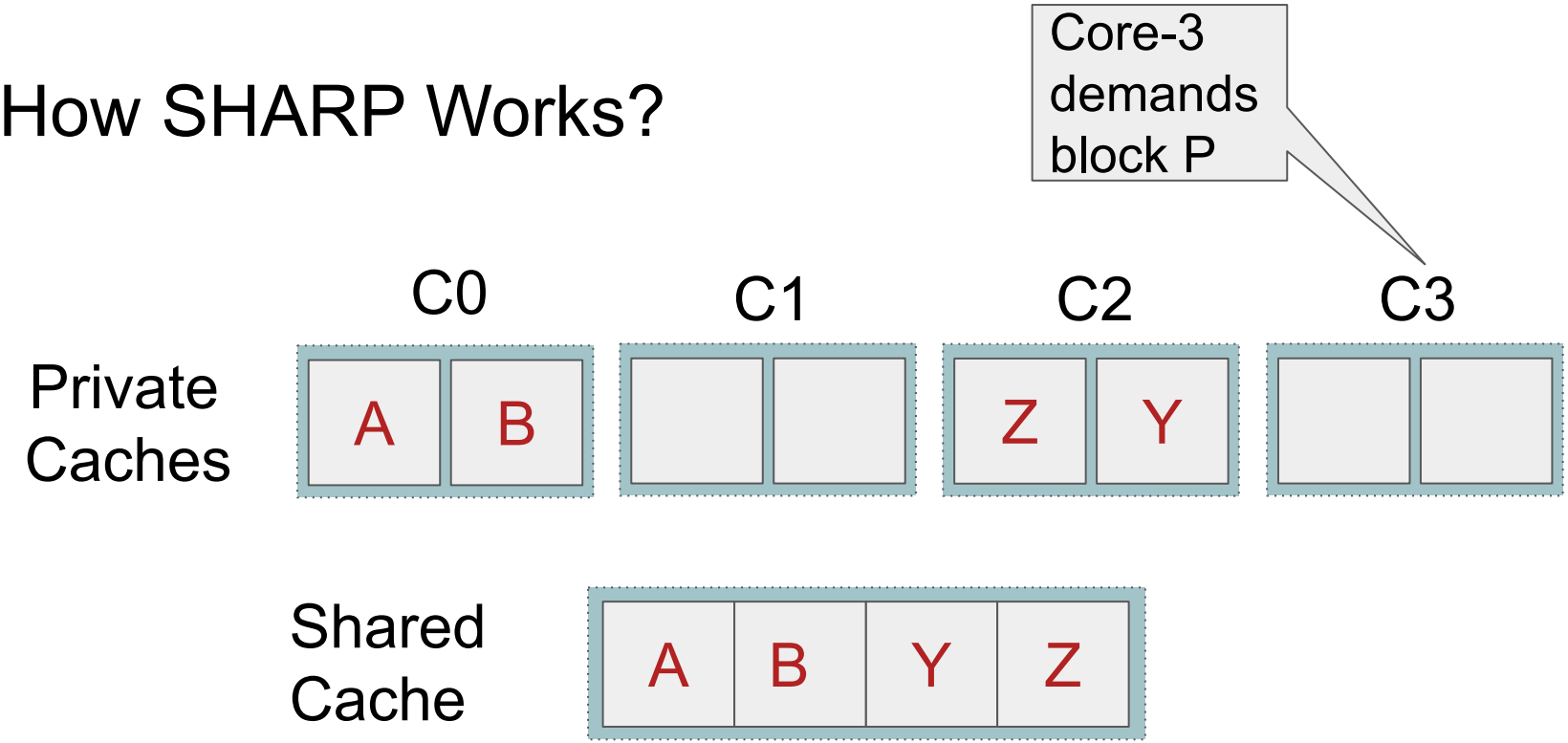

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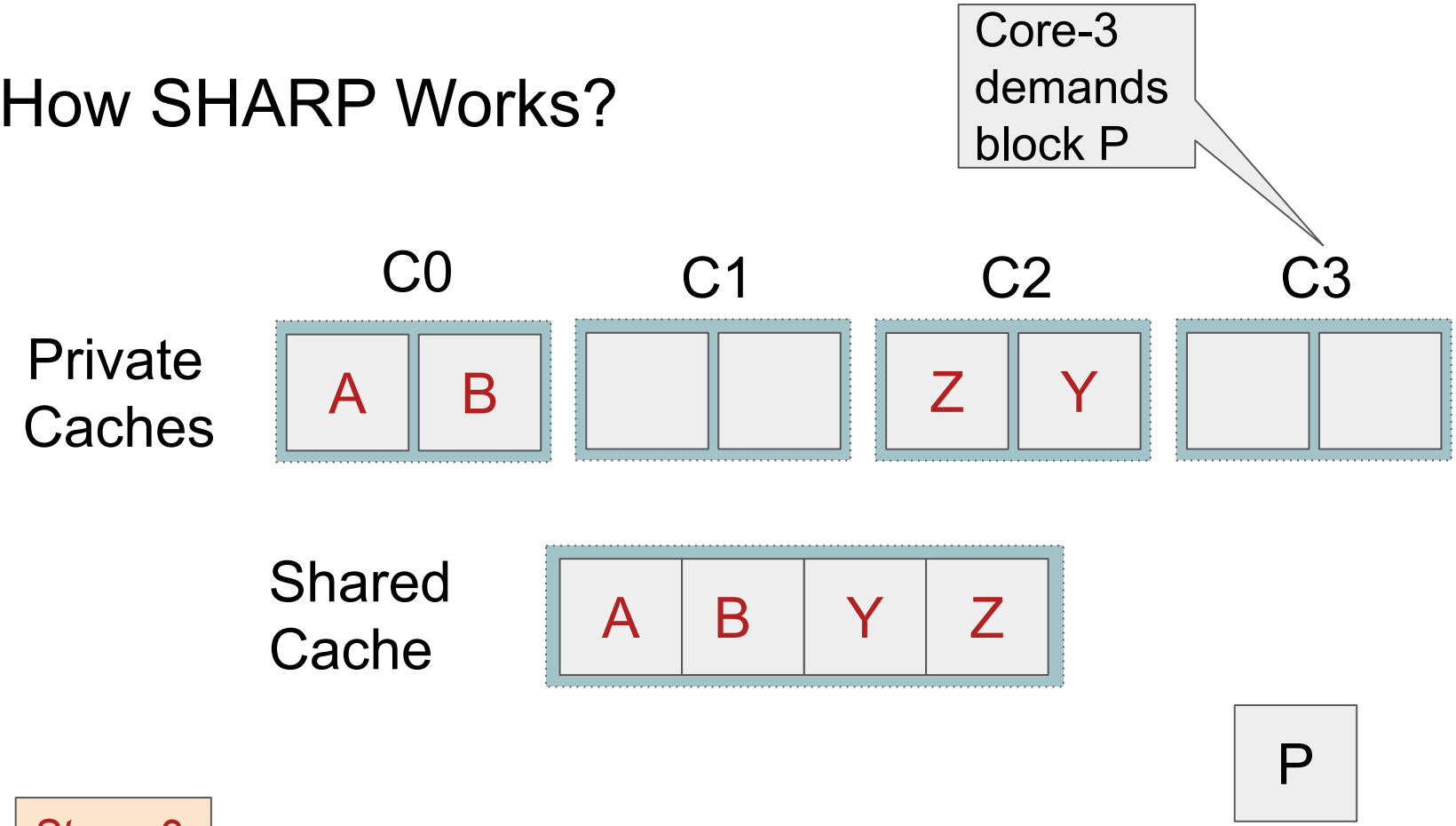

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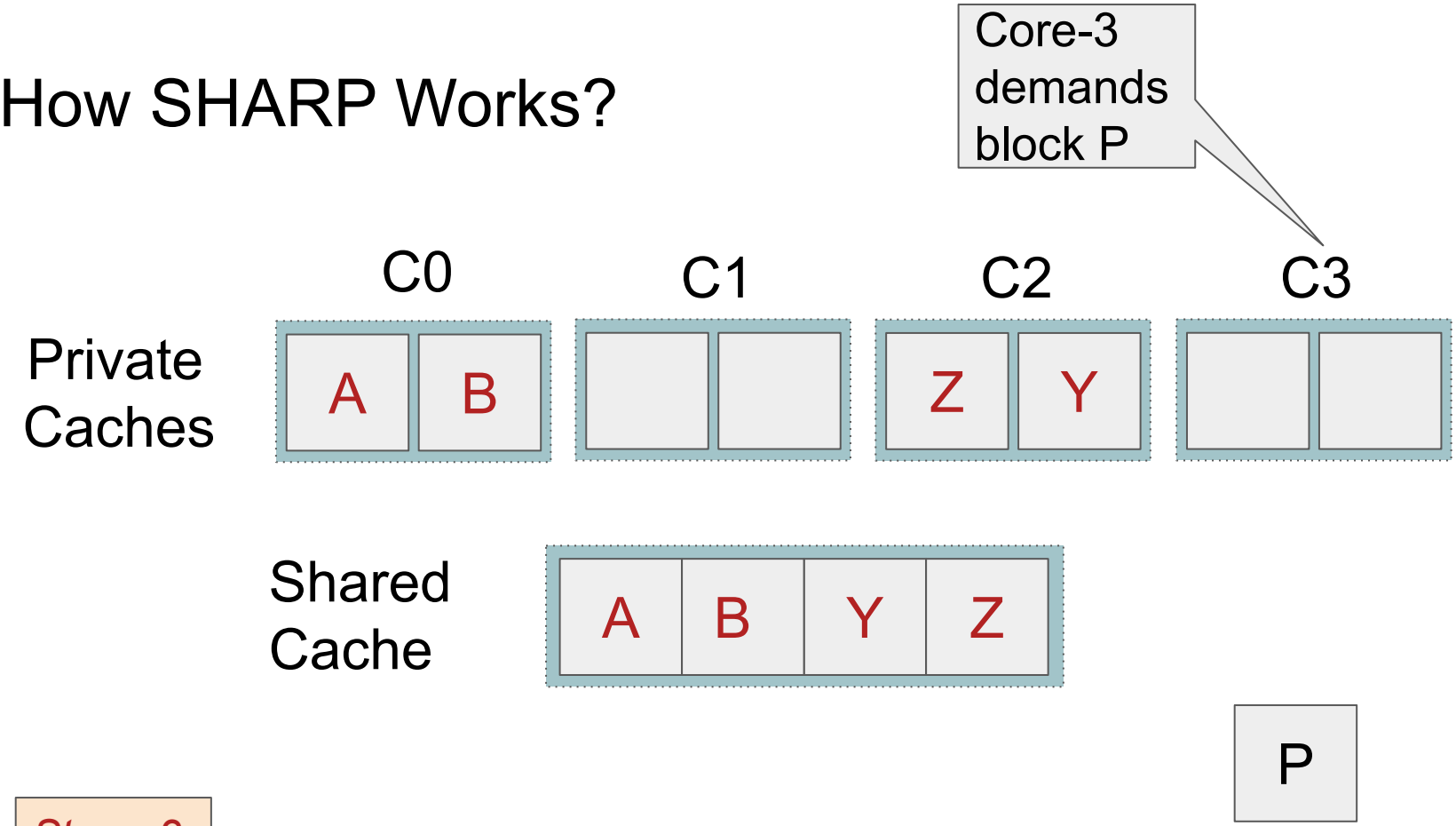

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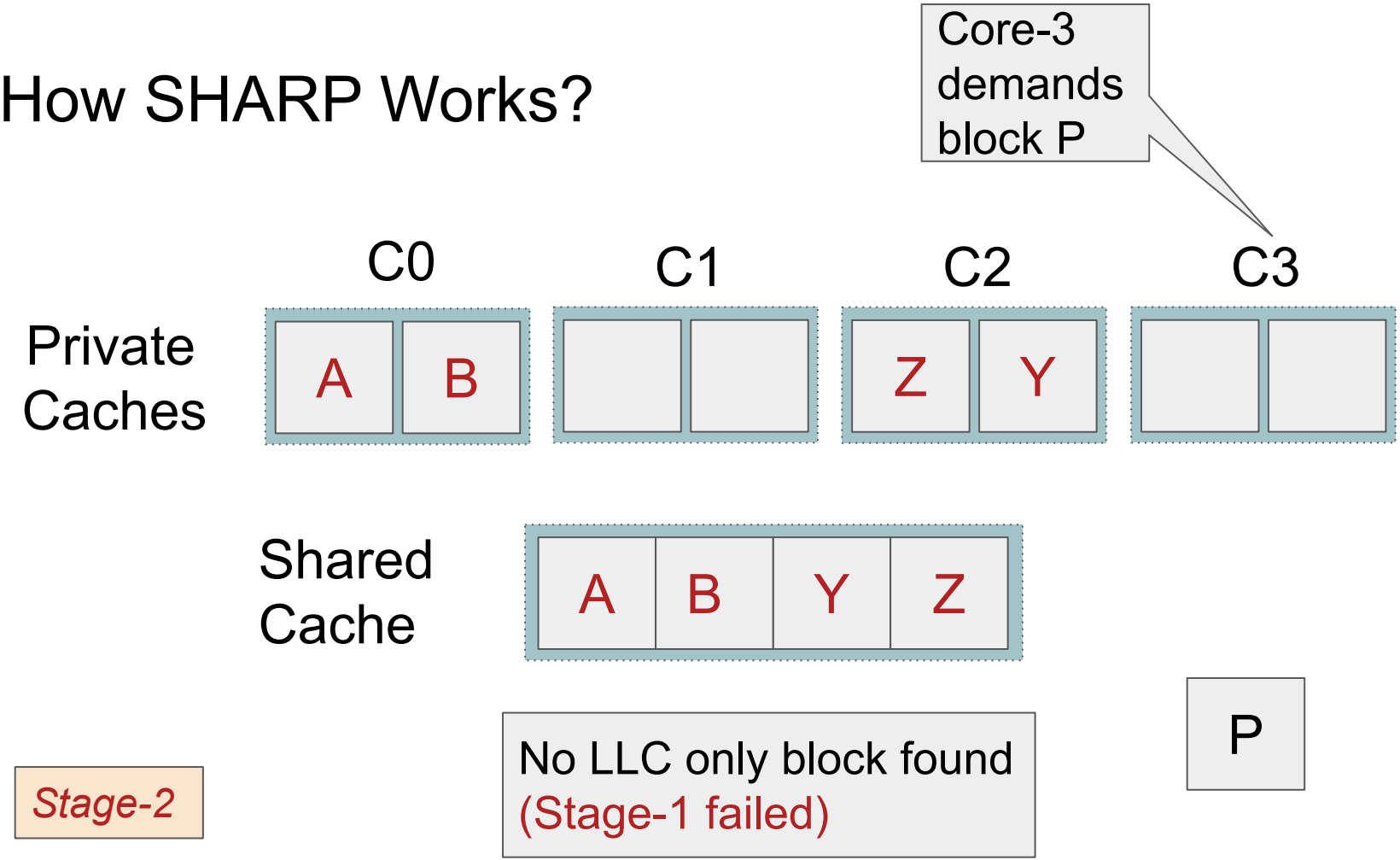

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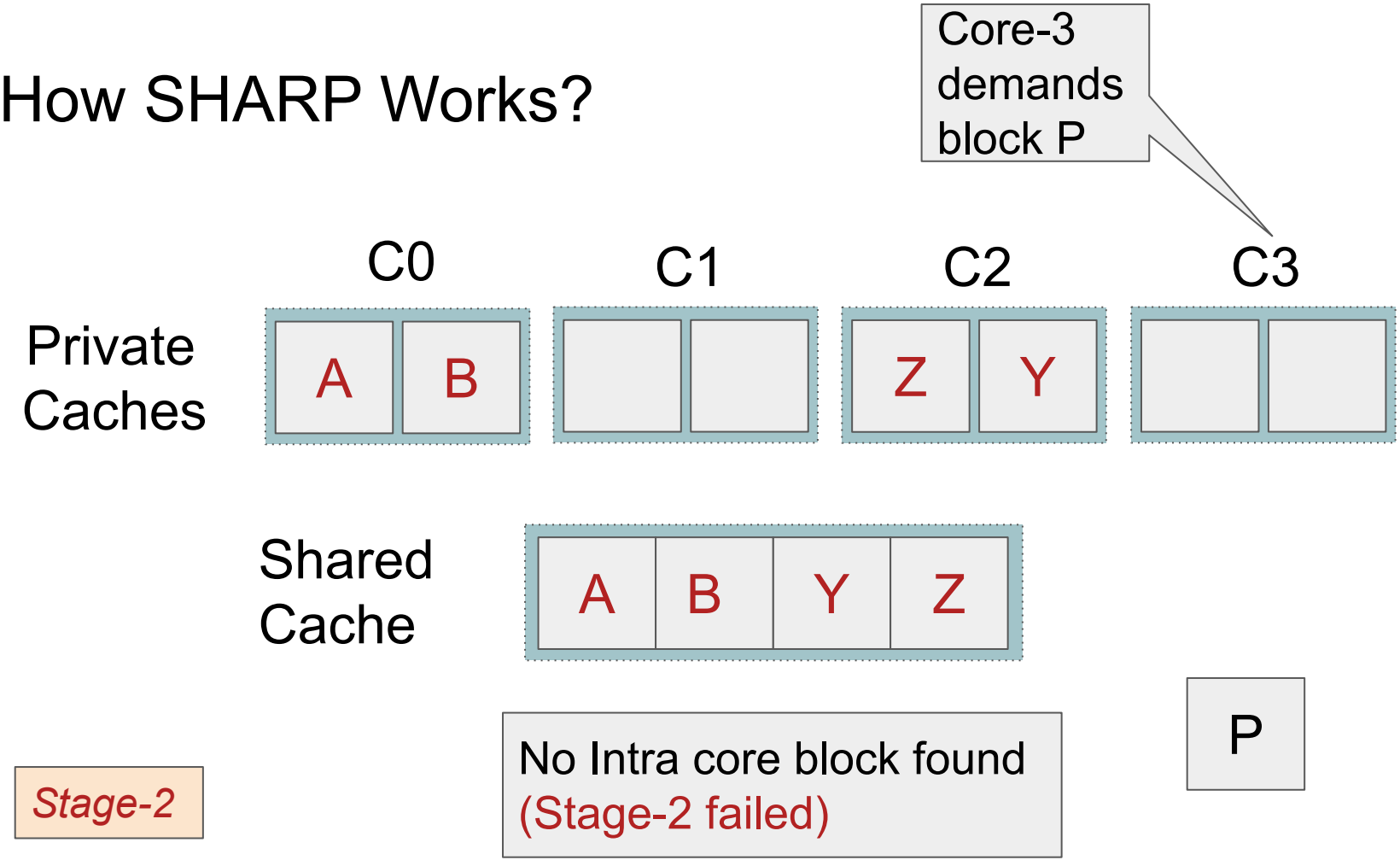

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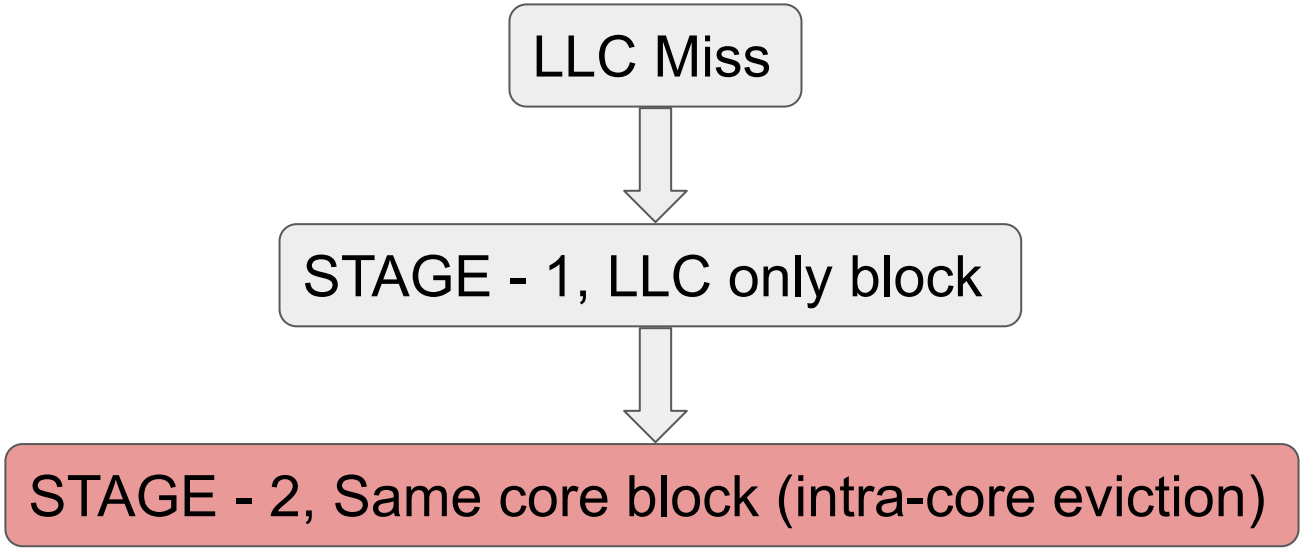

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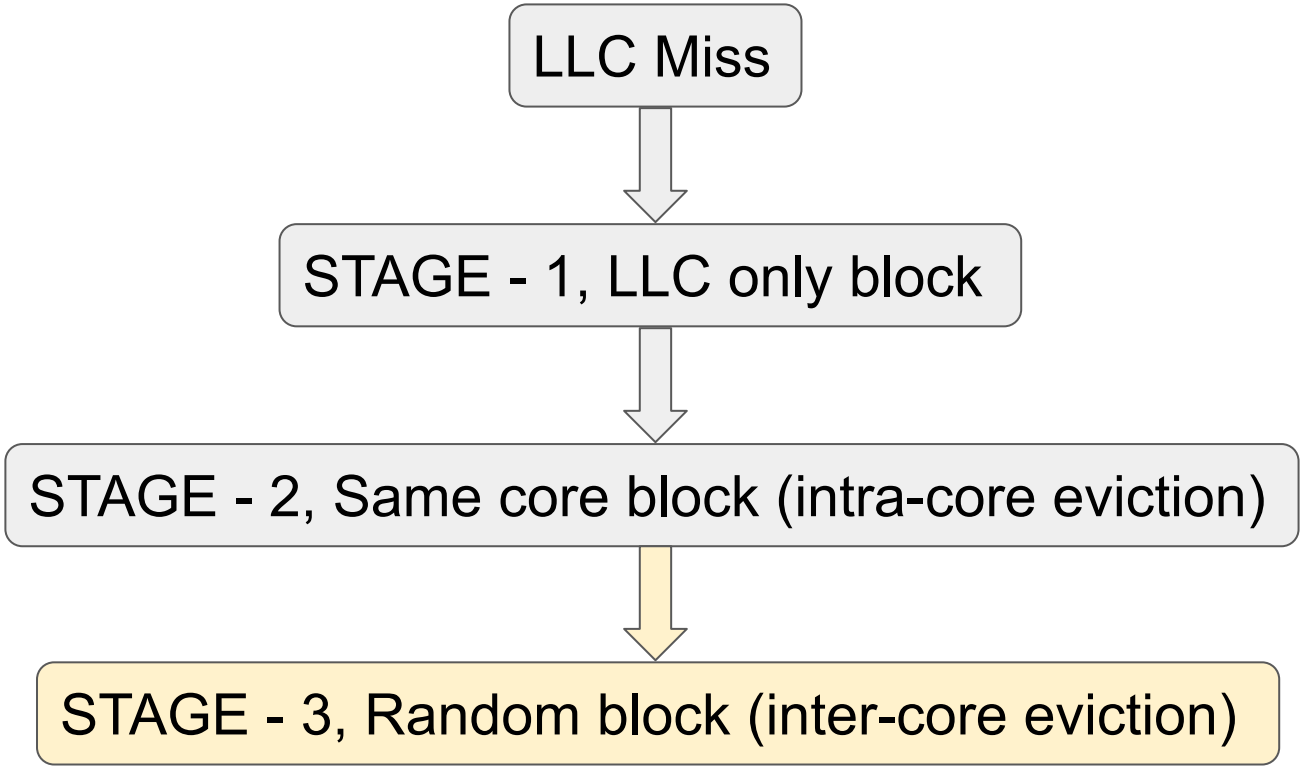

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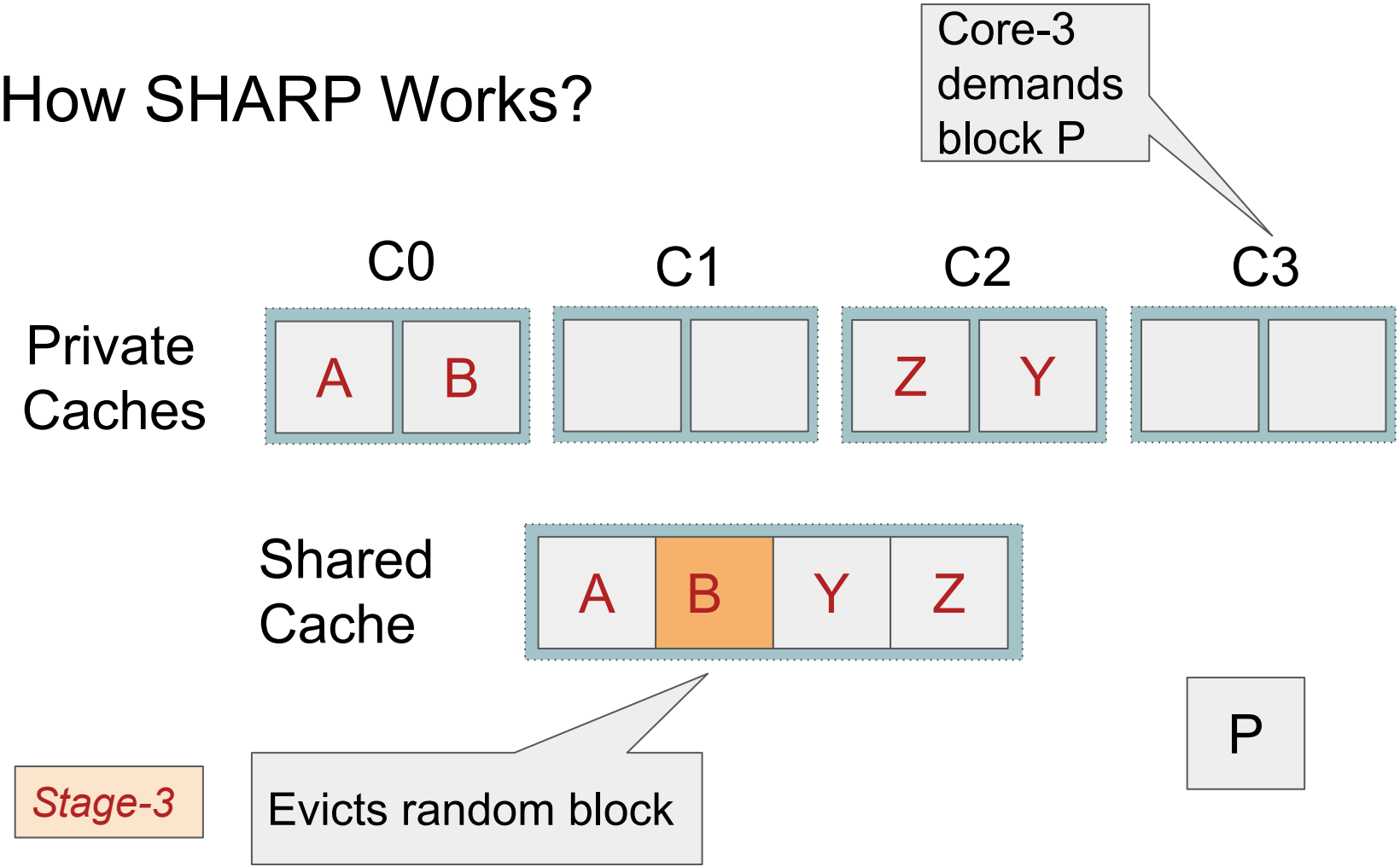

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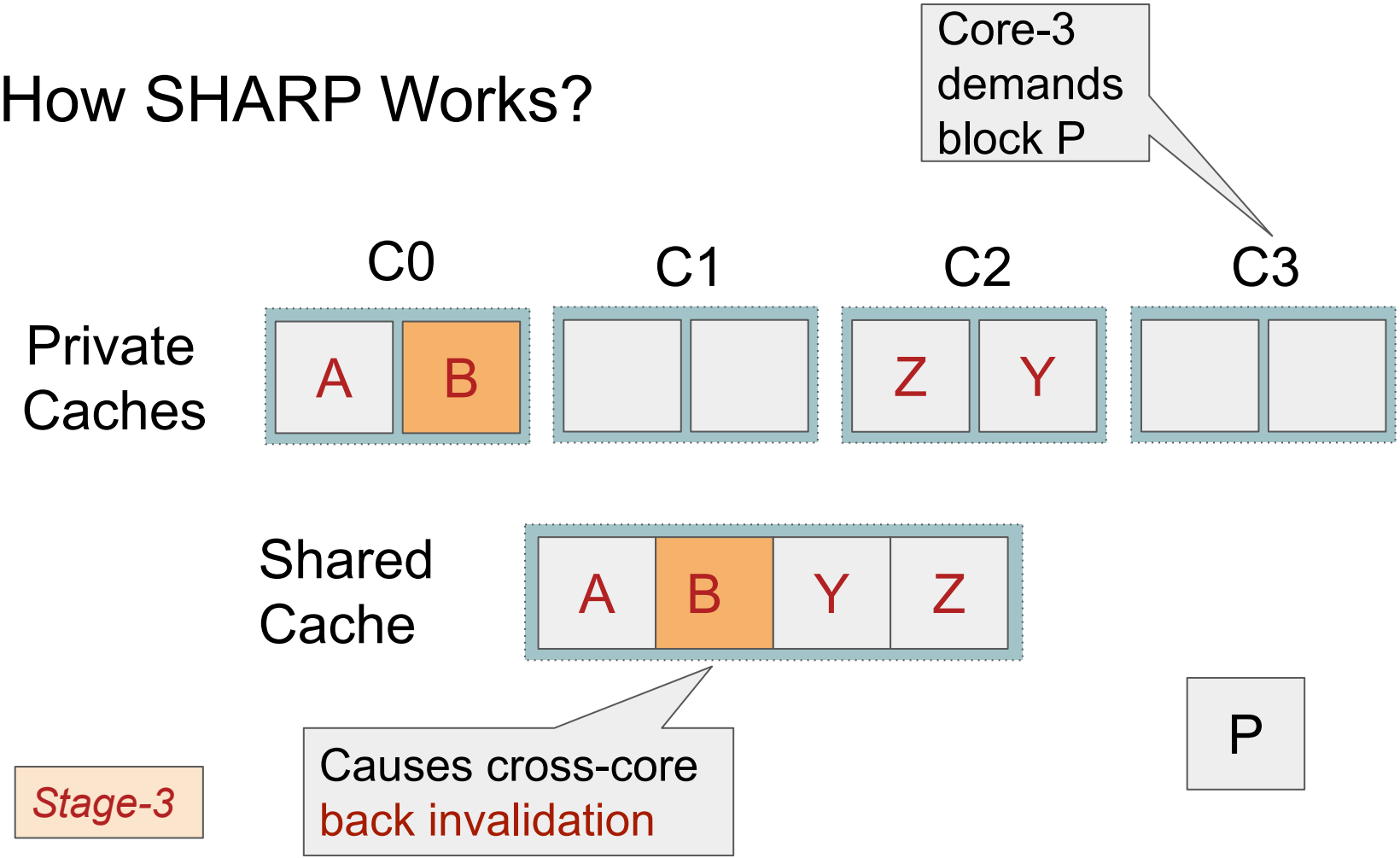

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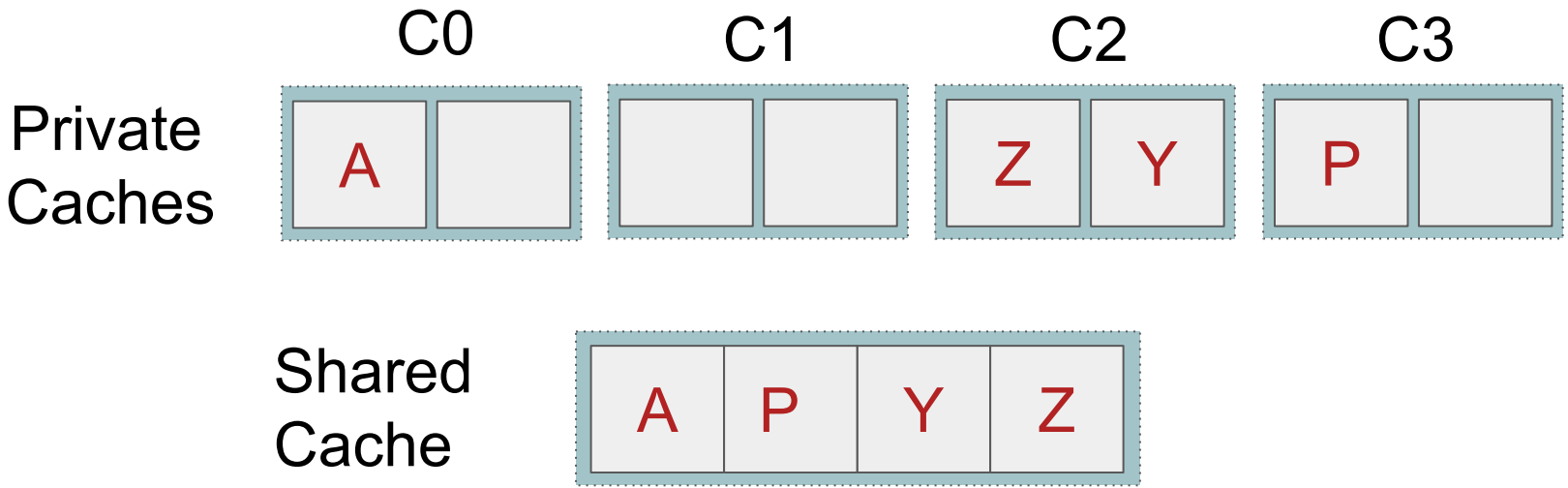

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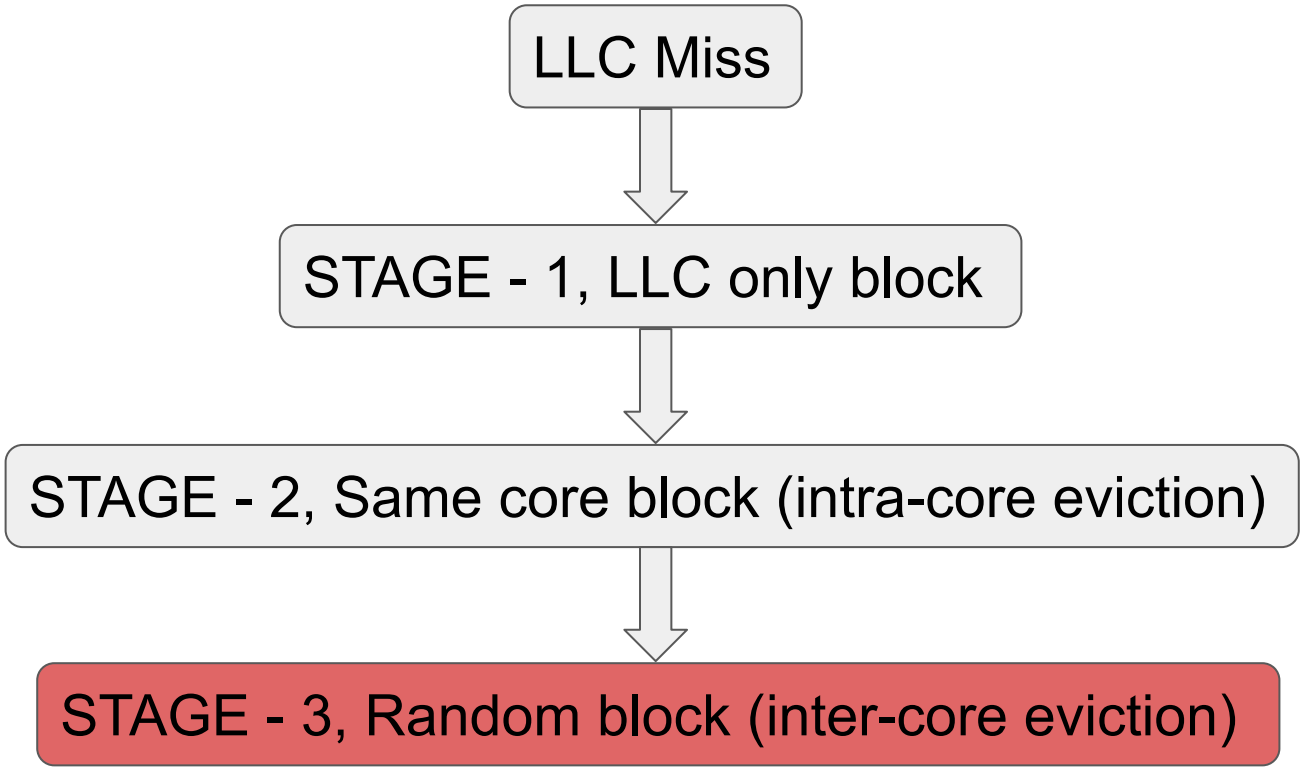

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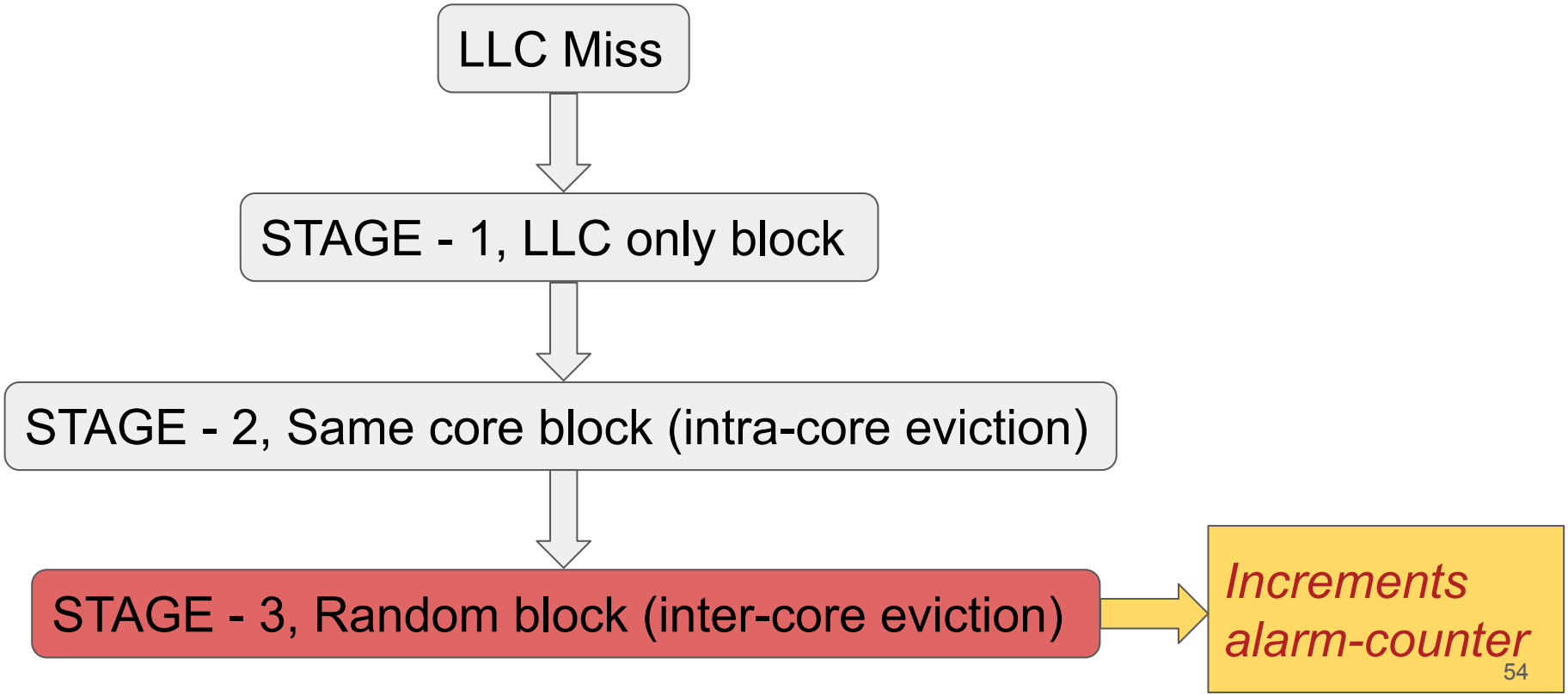

SHARP Alarm Counter

Counter per core

SHARP Alarm Counter

Counter per core

Increments on inter-core eviction

SHARP Alarm Counter

Counter per core

Increments on inter-core eviction

For 1 billion cycles, the threshold value is 2000

SHARP Alarm Counter

Counter per core

Increments on inter-core eviction

For 1 billion cycles, the threshold value is 2000

On exceeding threshold, SHARP triggers OS interrupt

Questions That We Ask?

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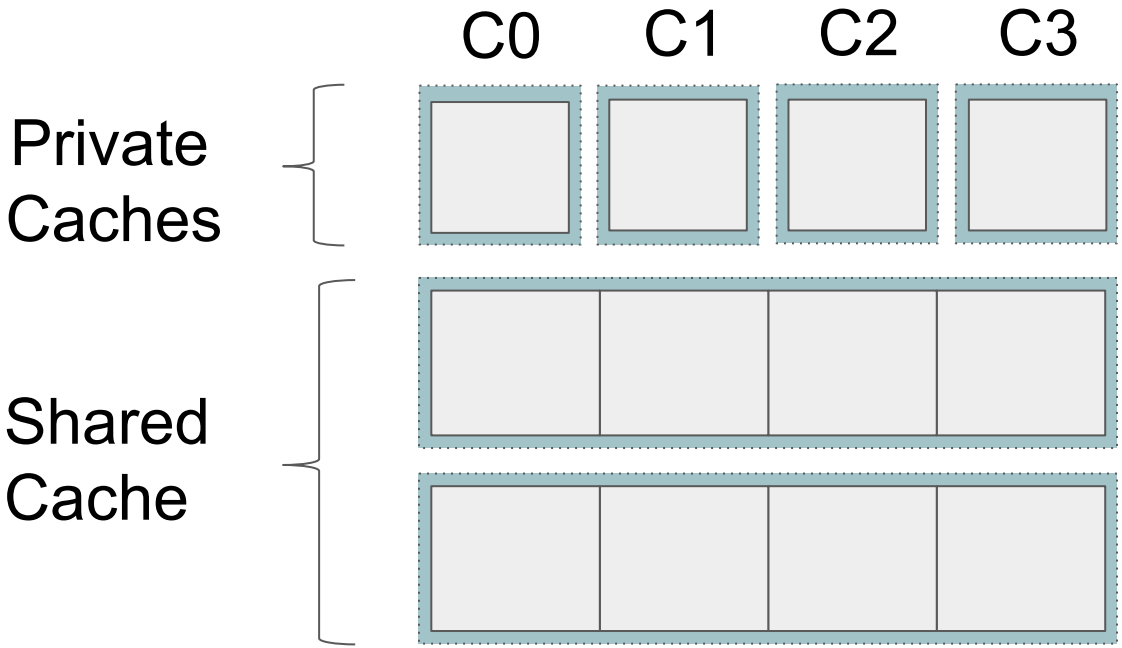
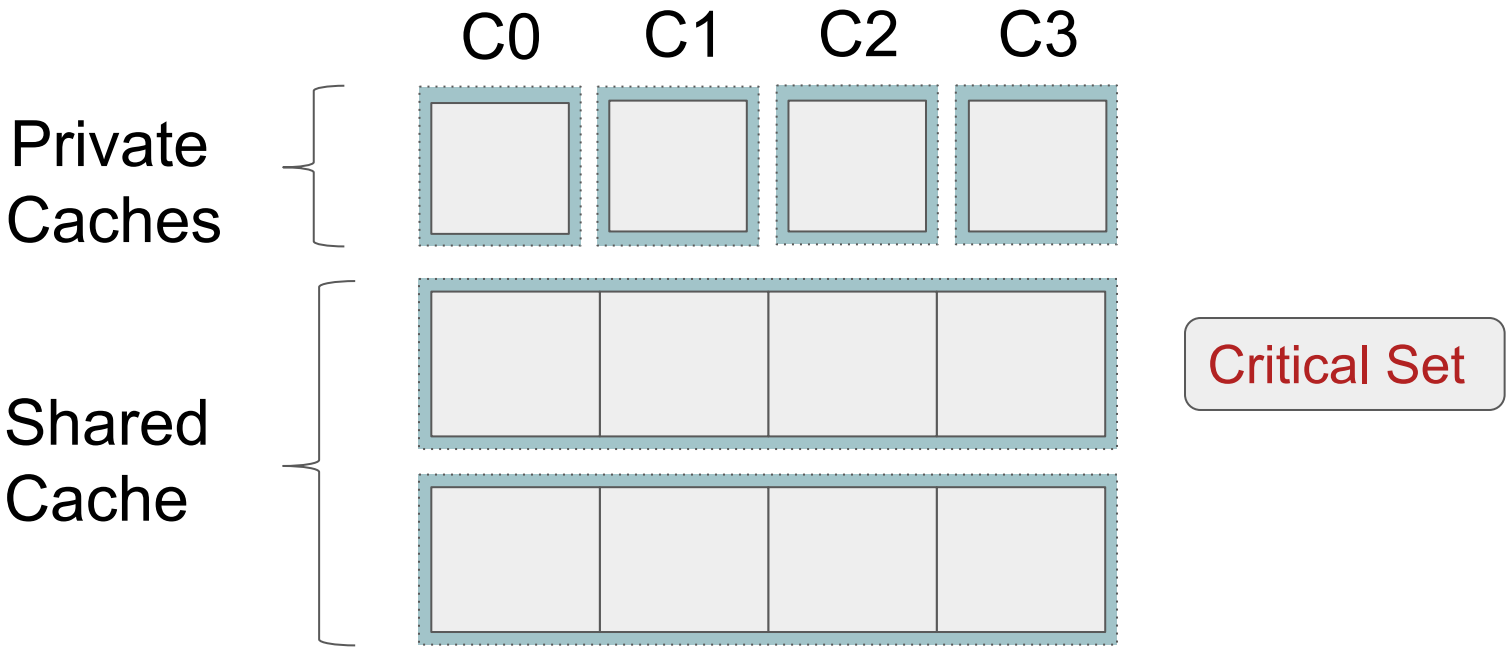
Does SHARP mitigate all attacks?

Prime+Reprime+Probe



Prime+Reprime+Probe



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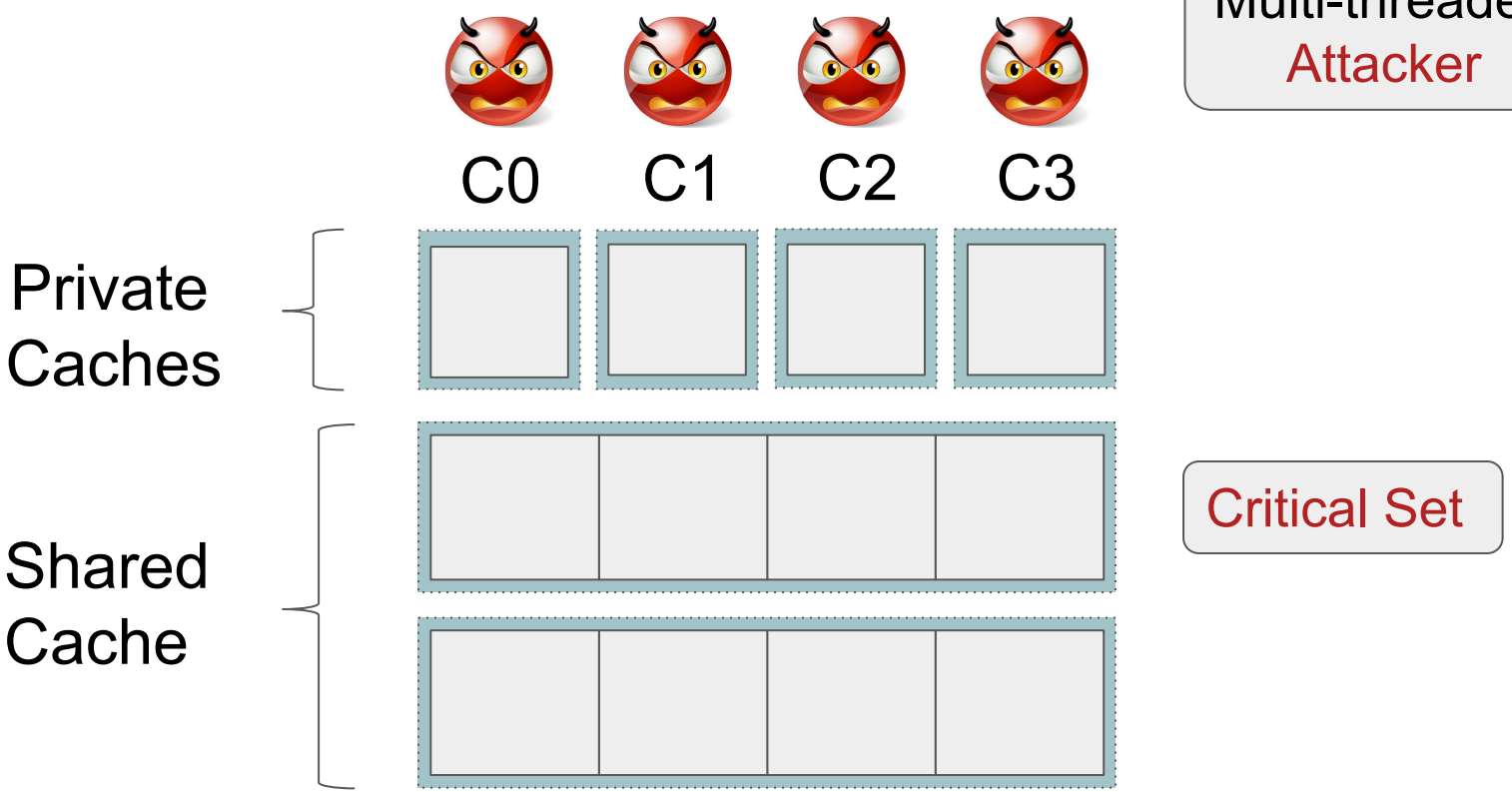

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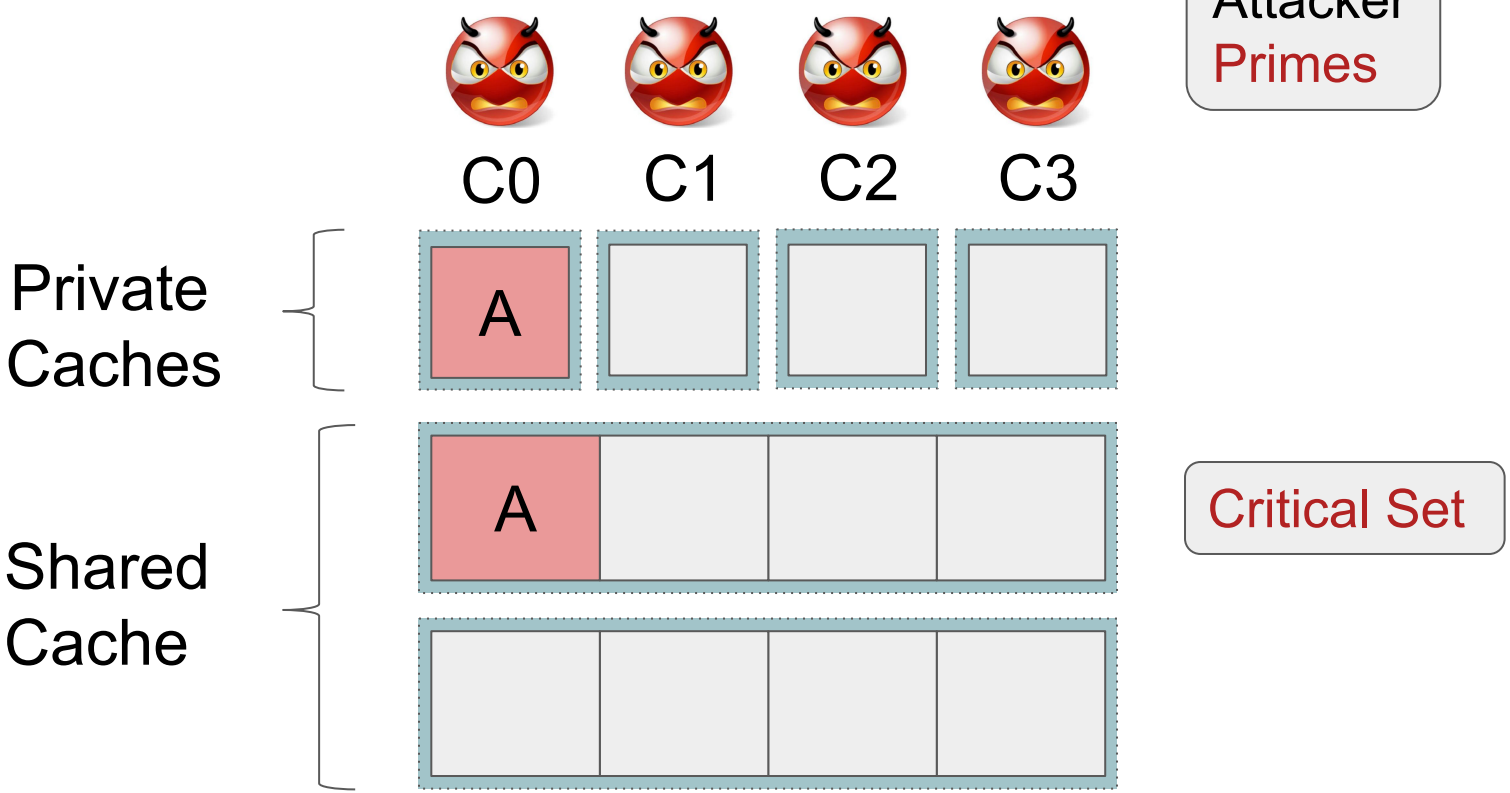

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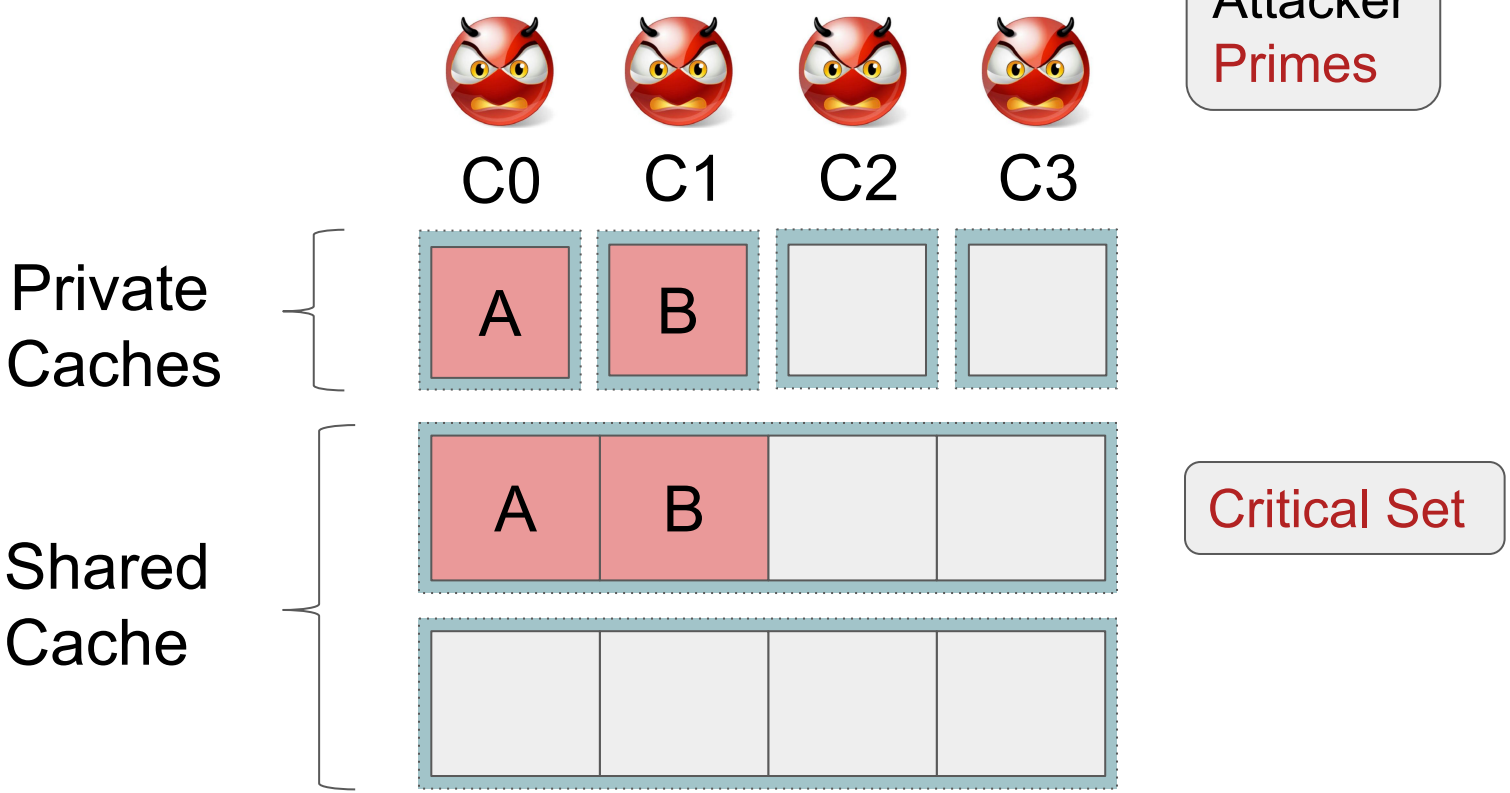

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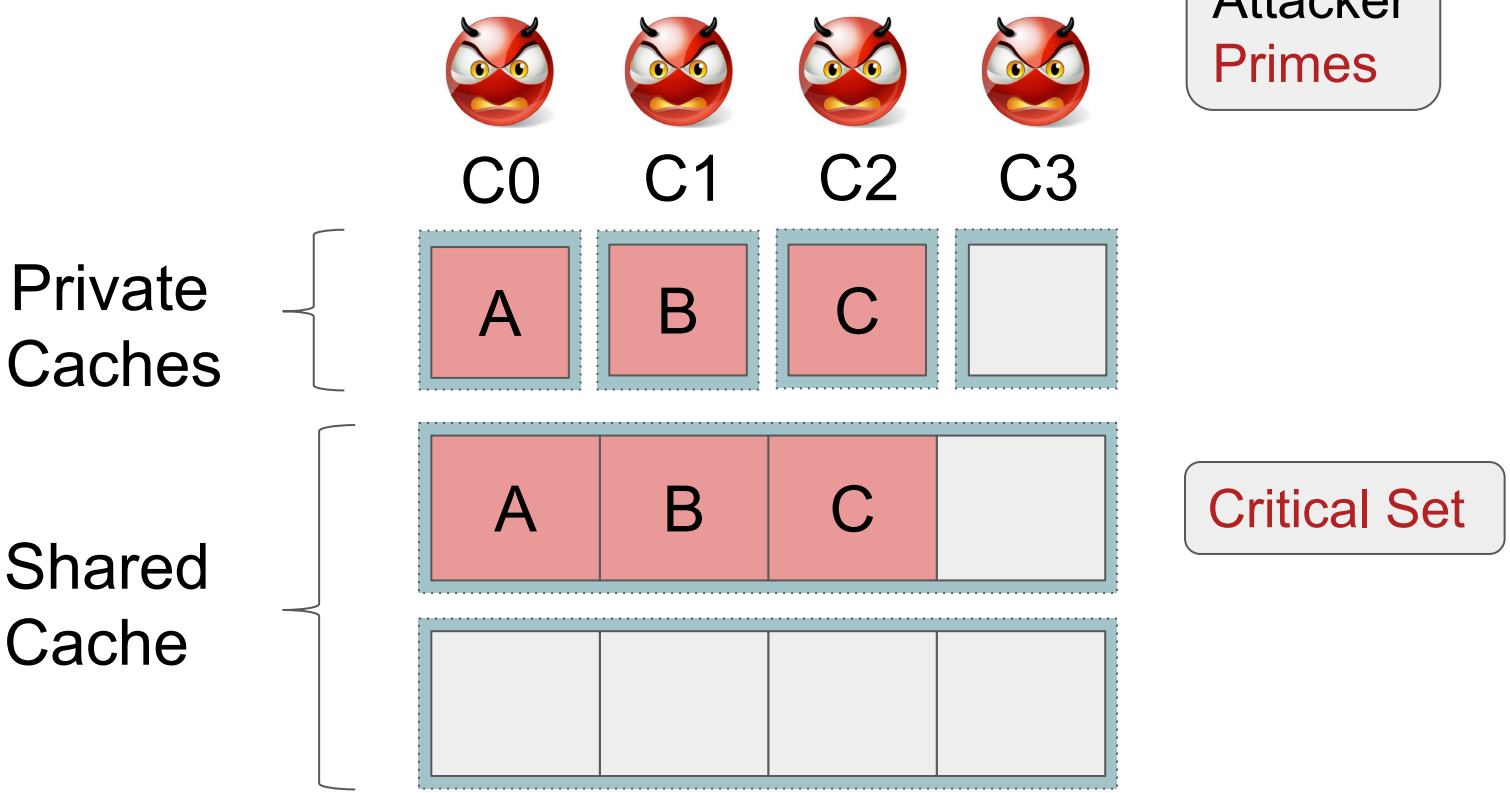

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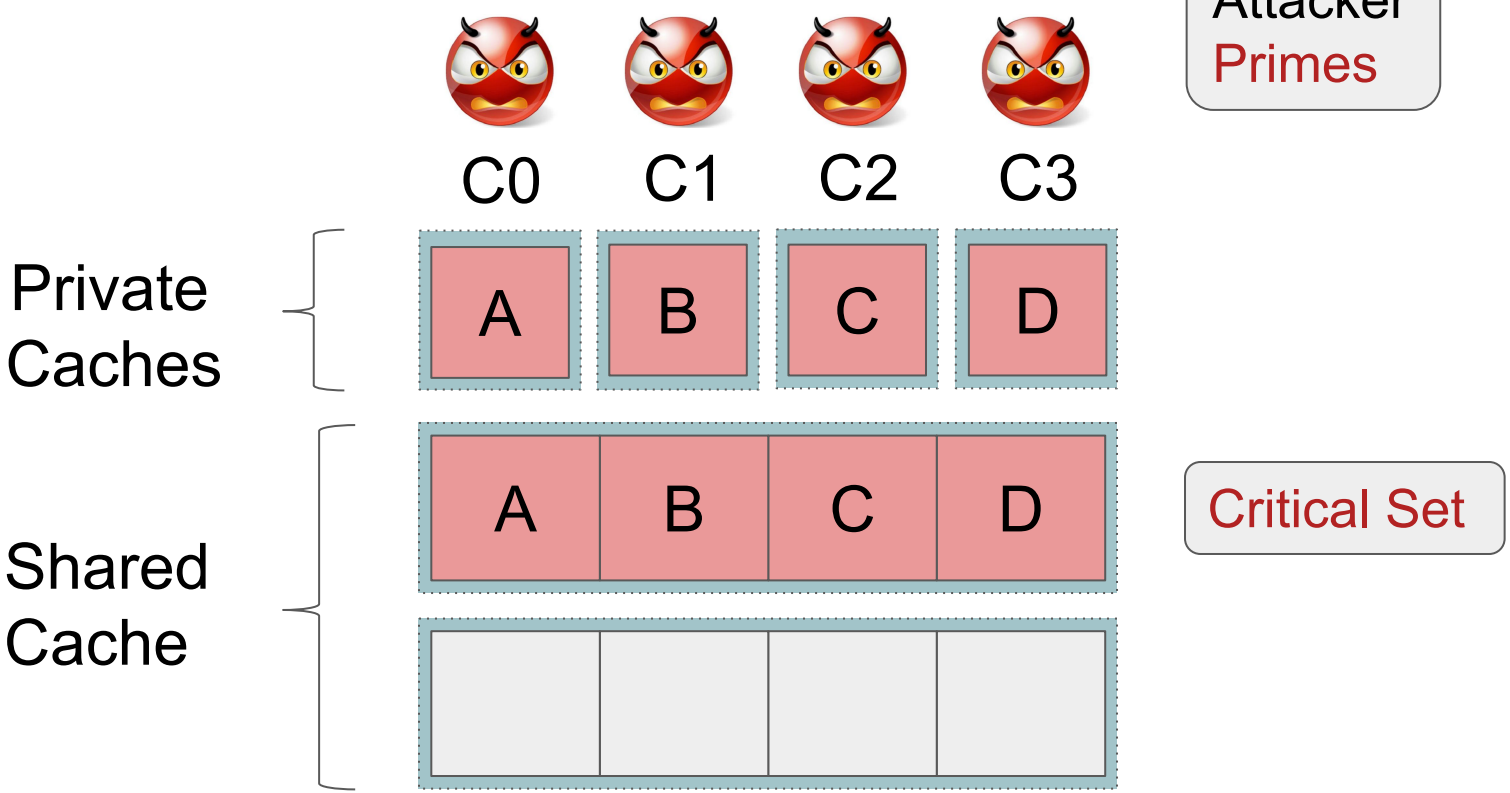

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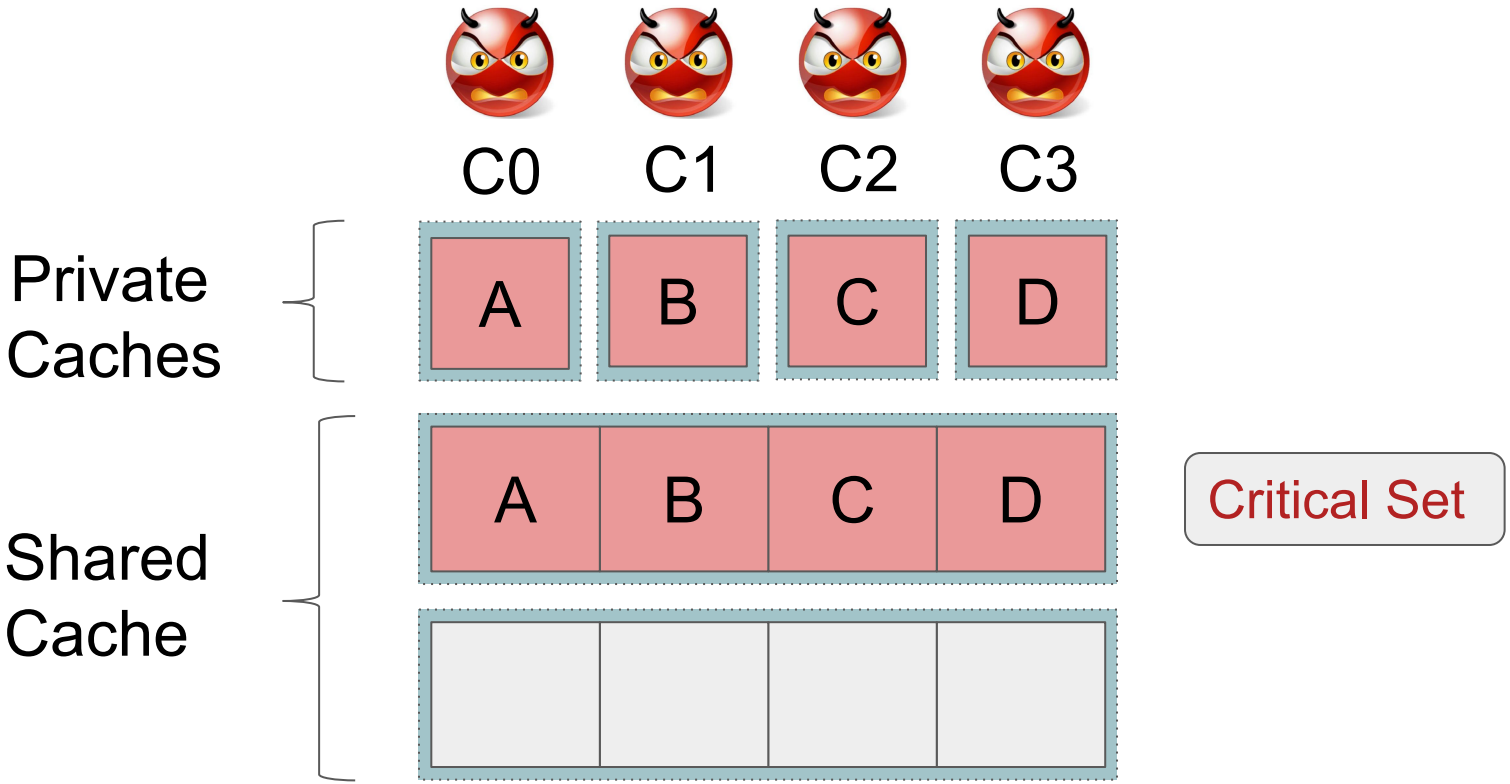

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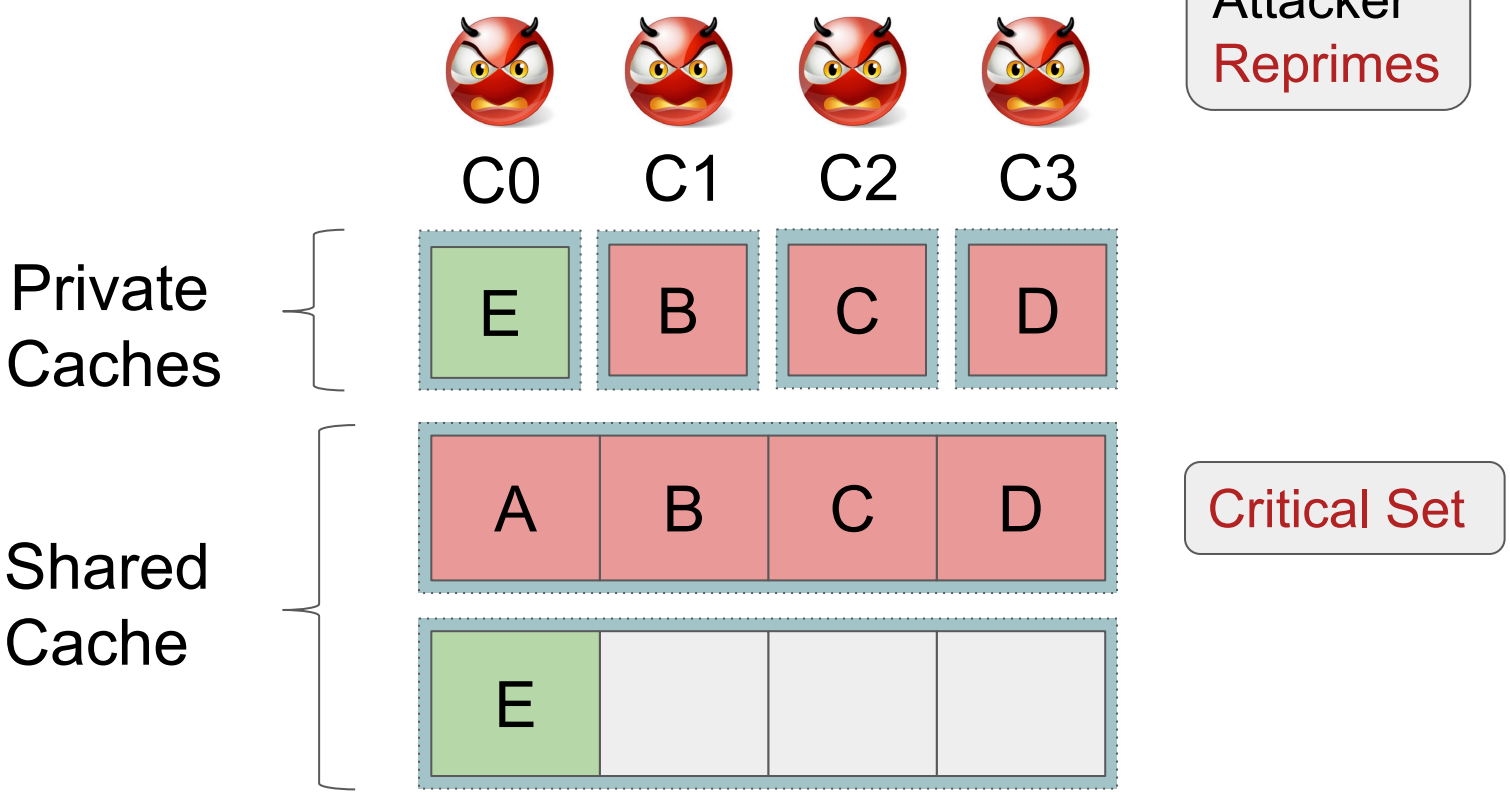

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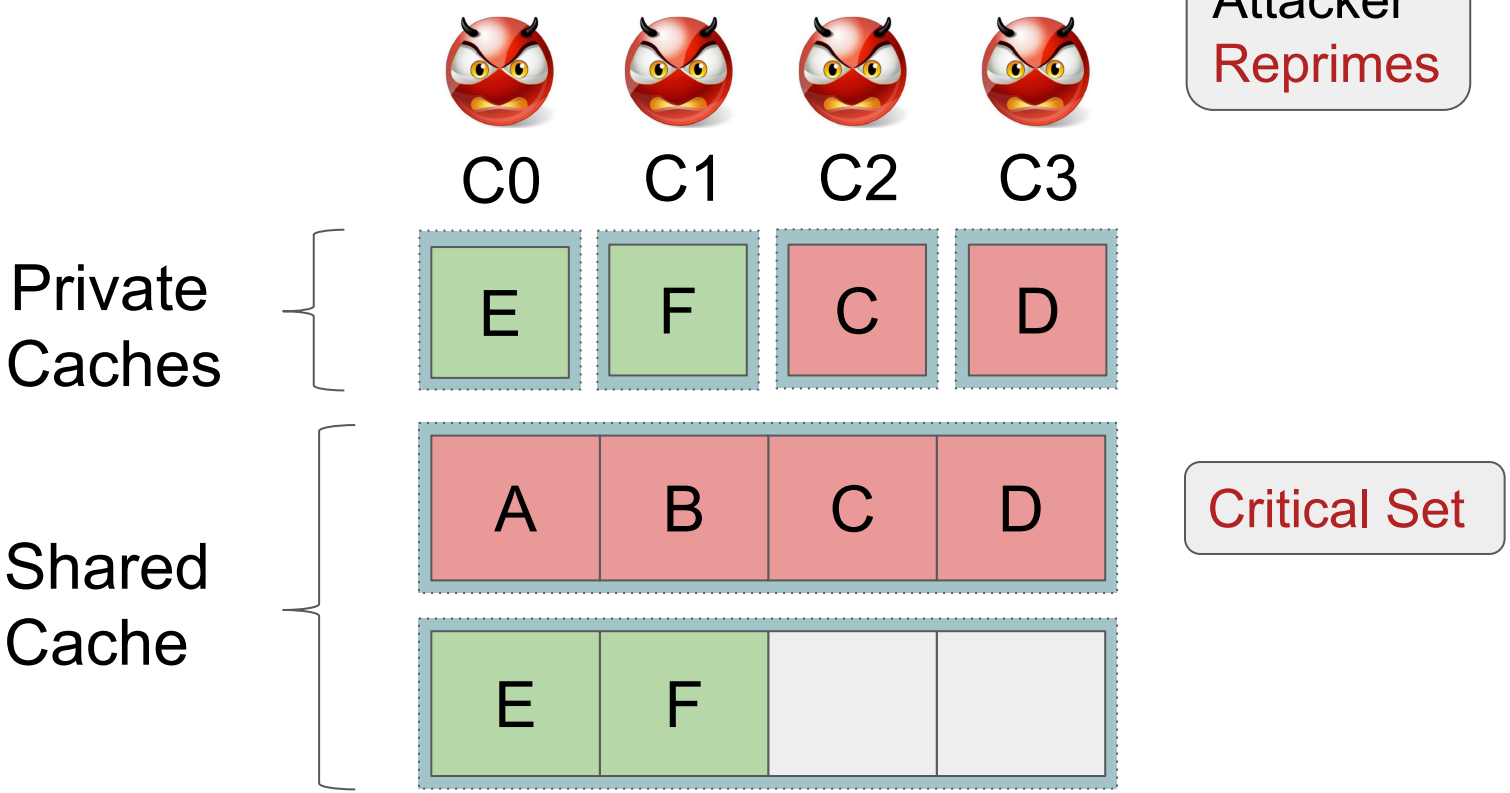

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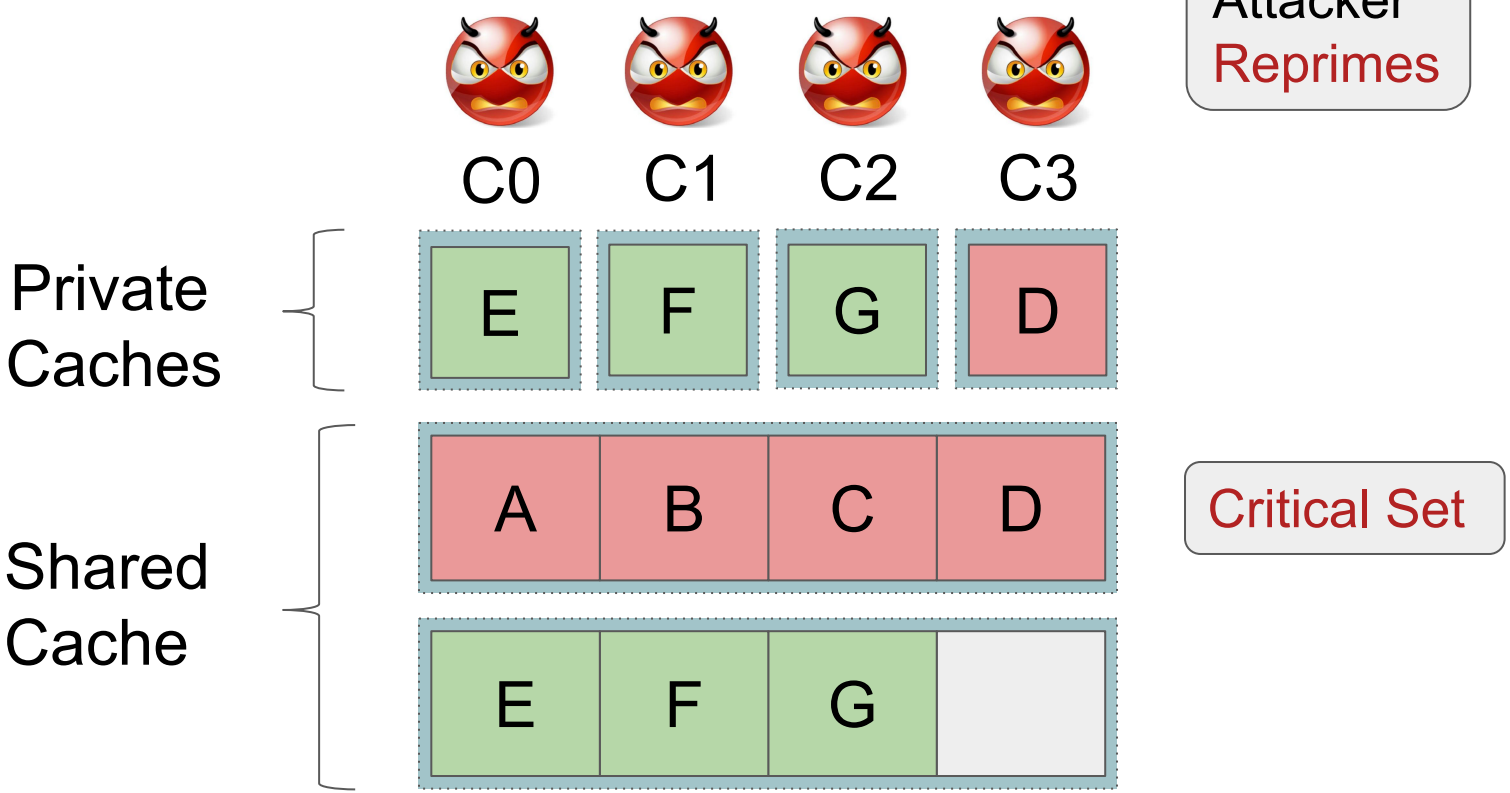
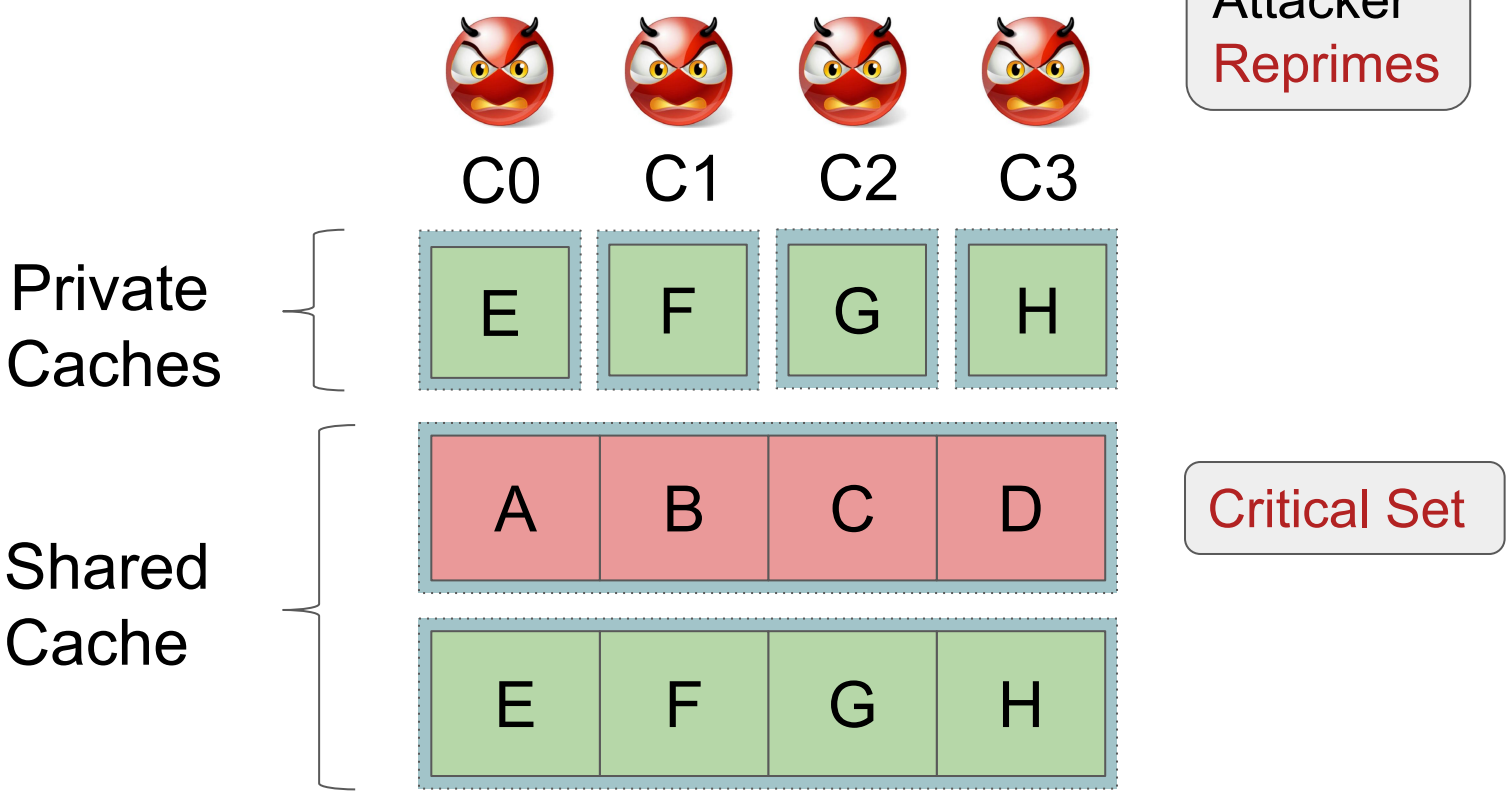


Prime+Reprime+Probe



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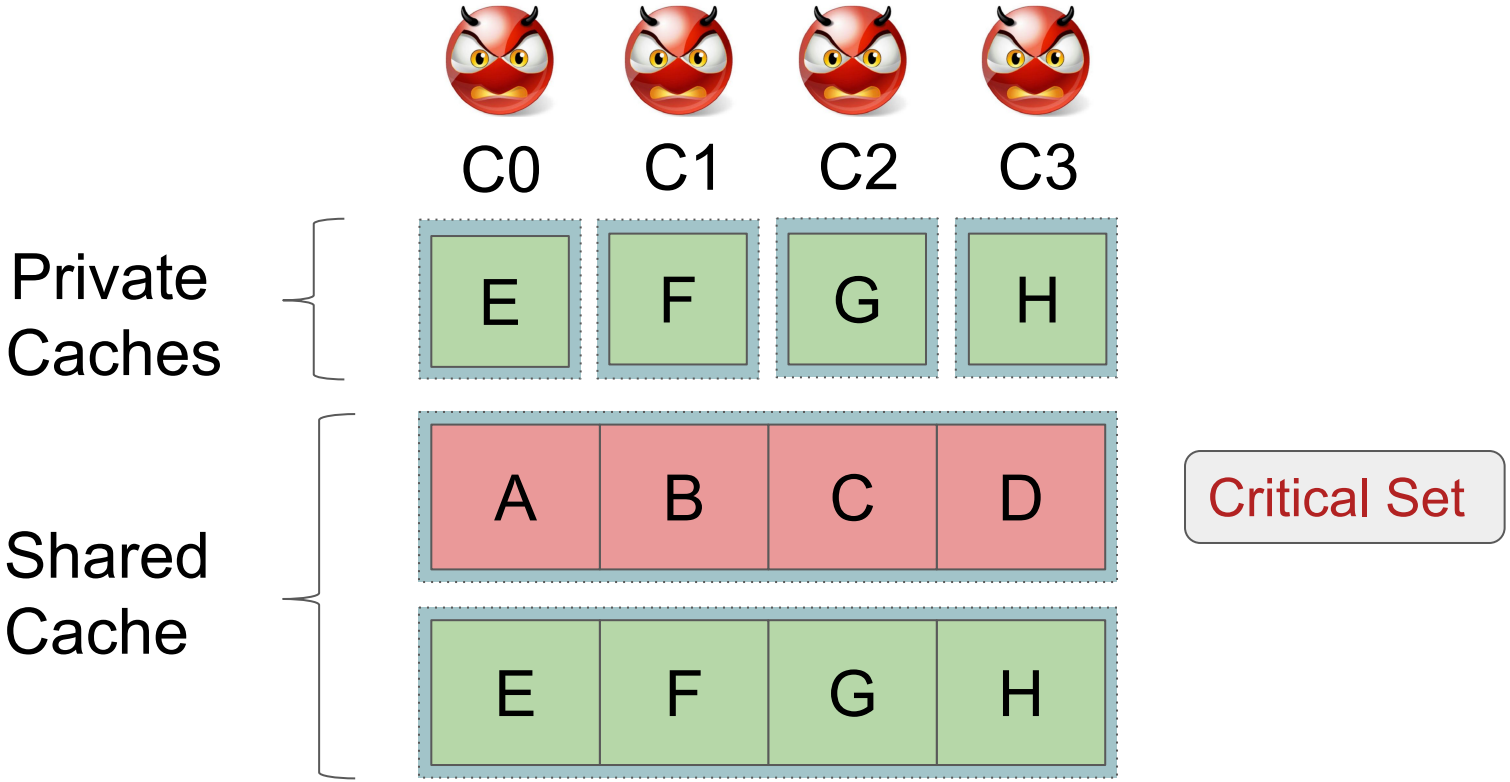

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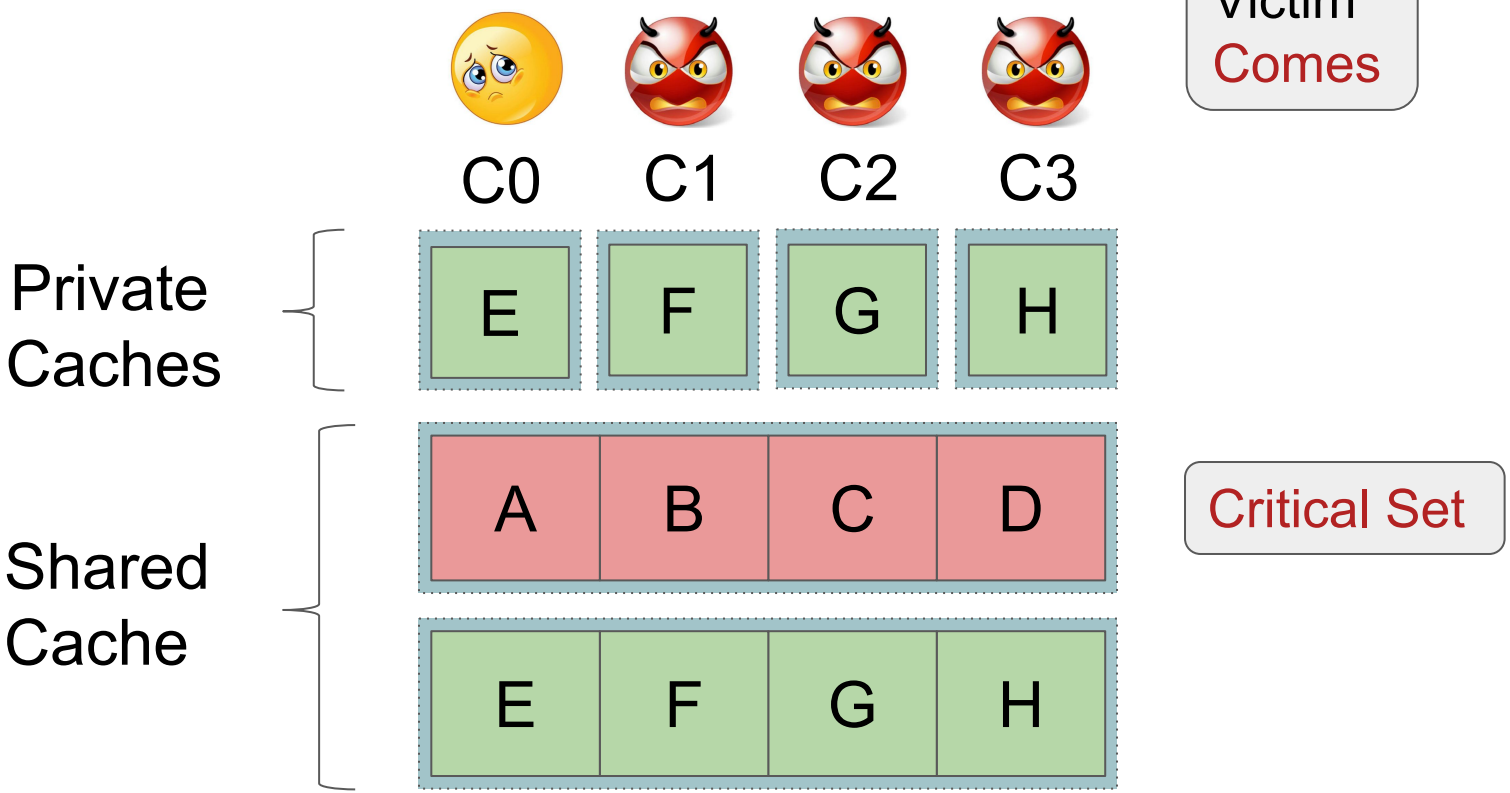

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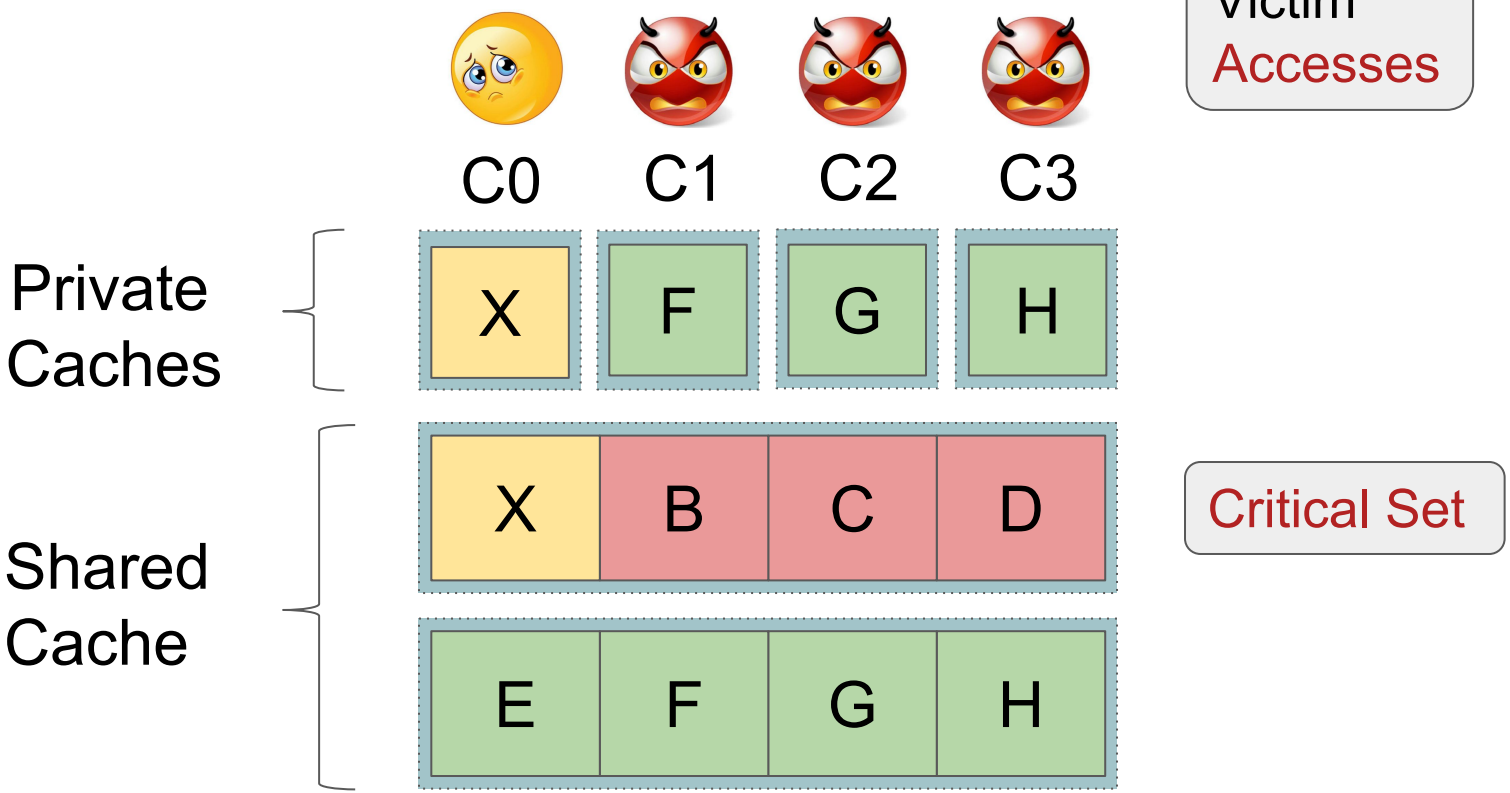

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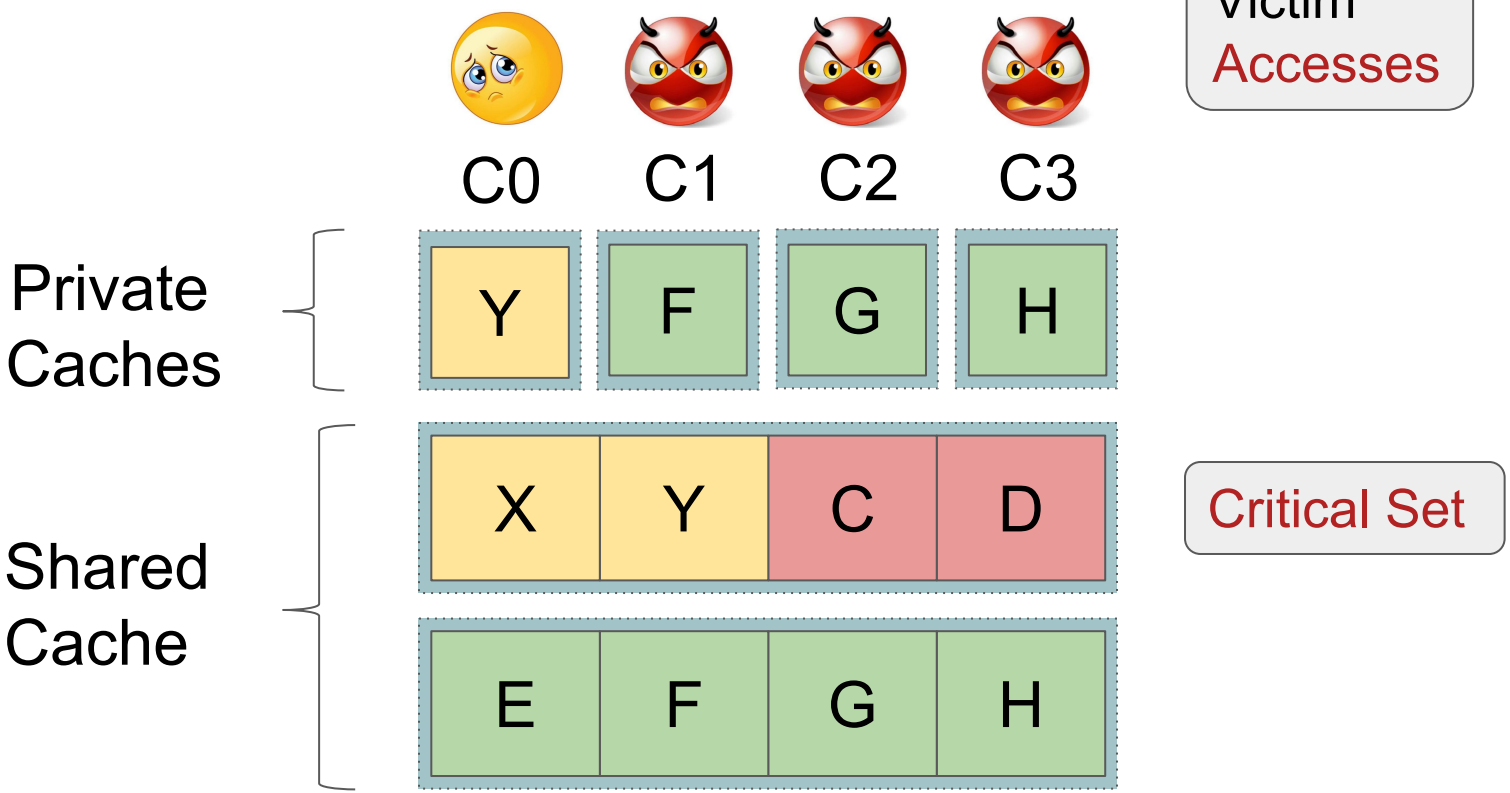

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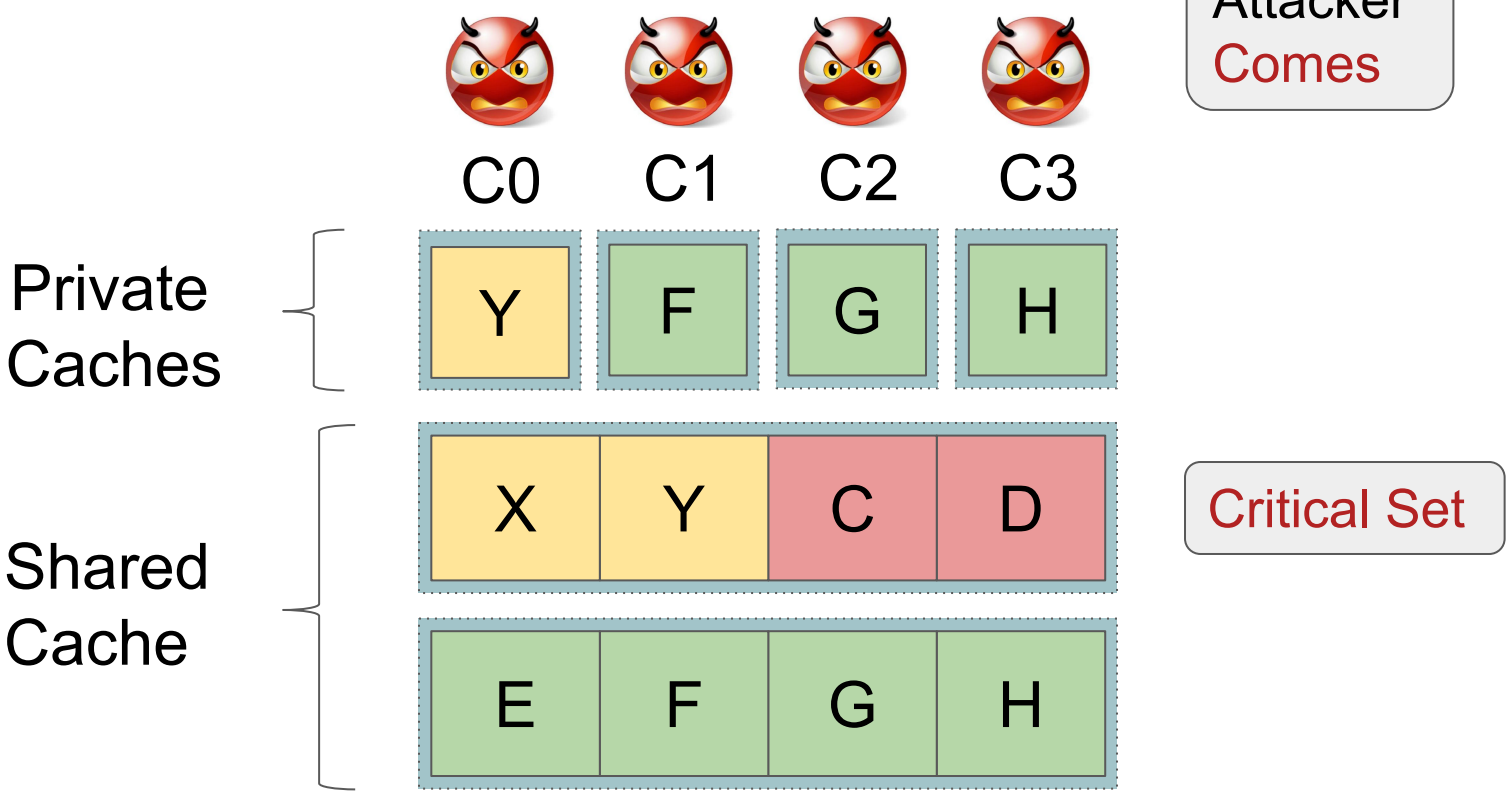

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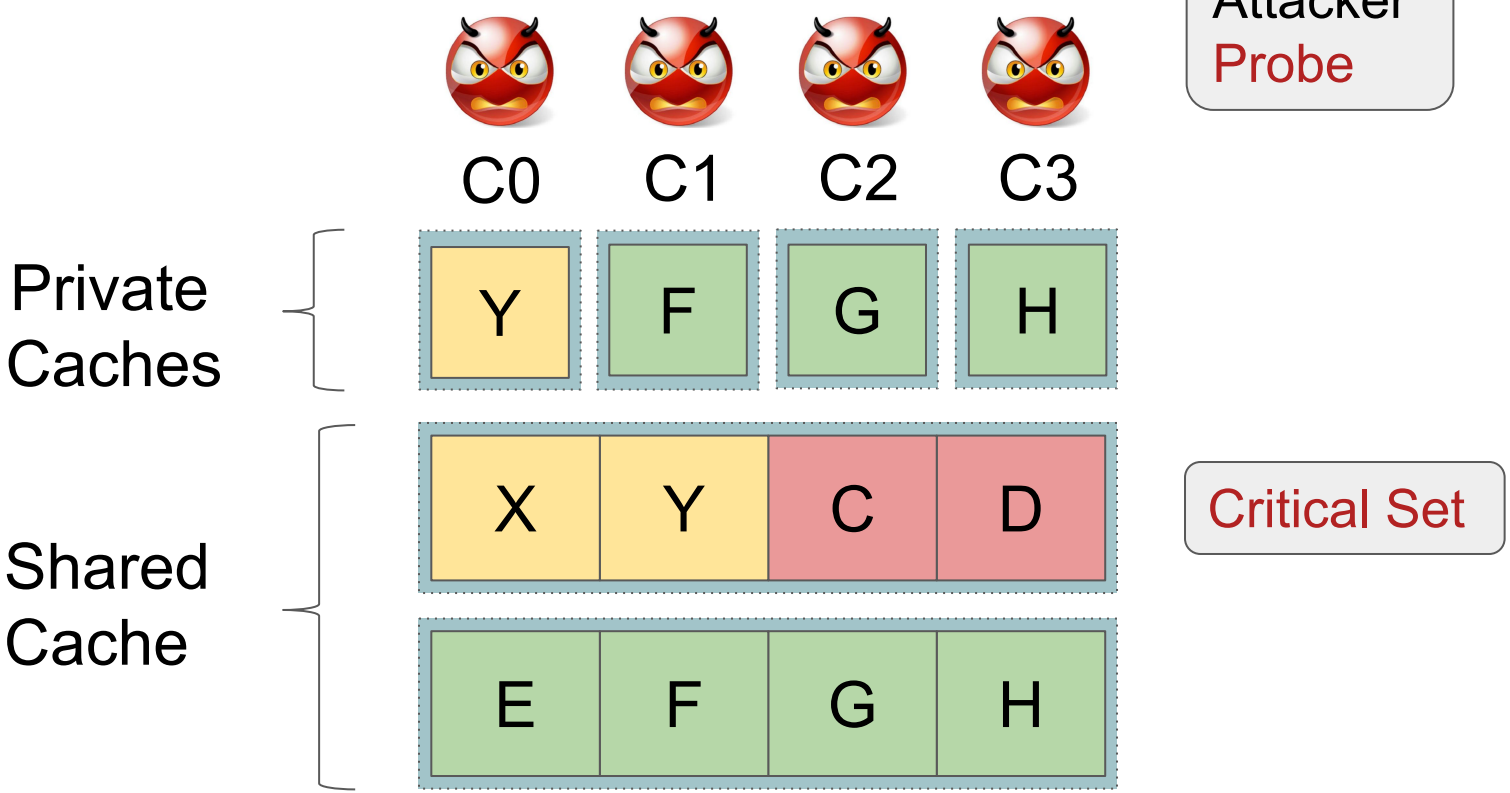

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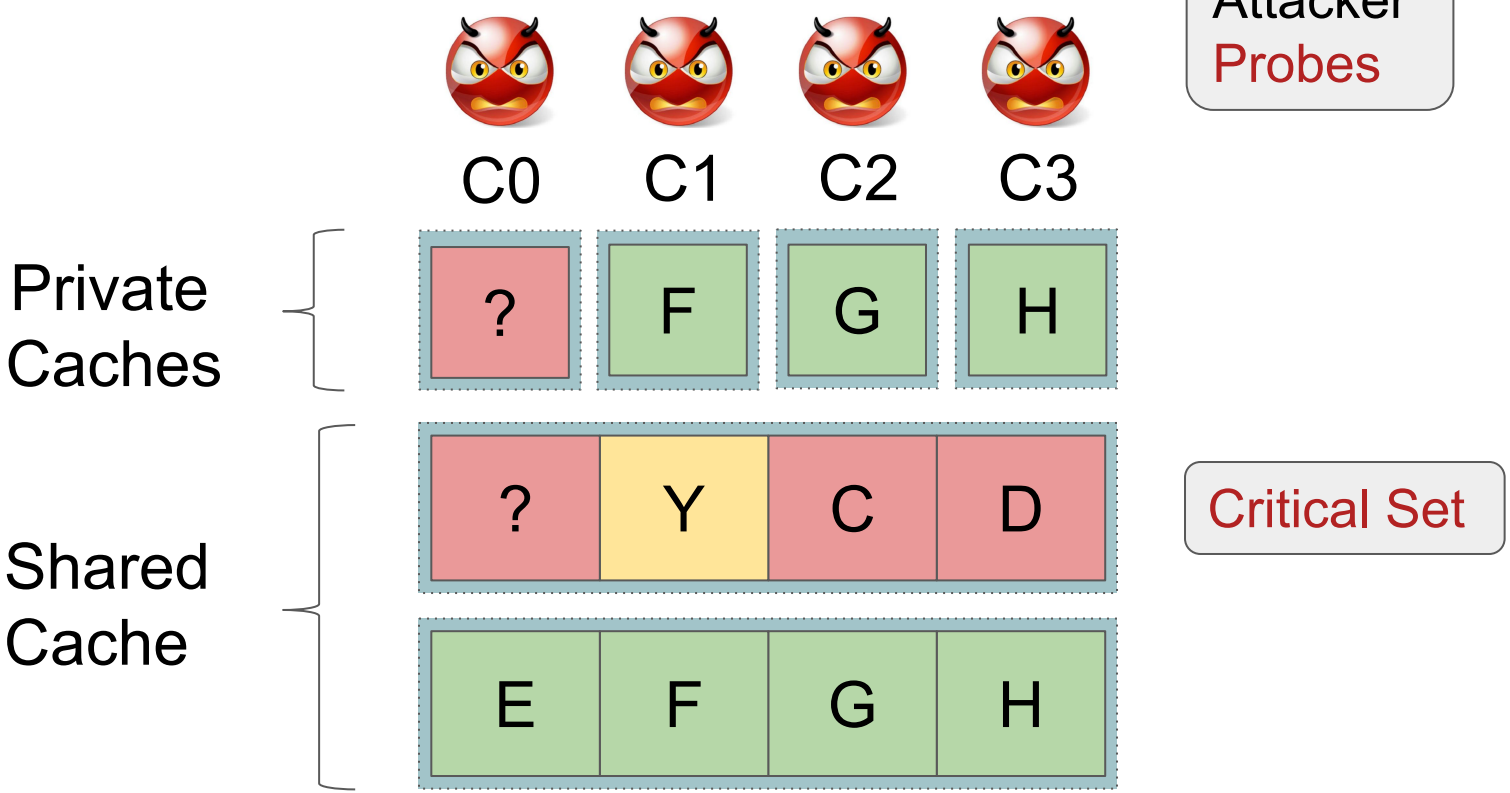

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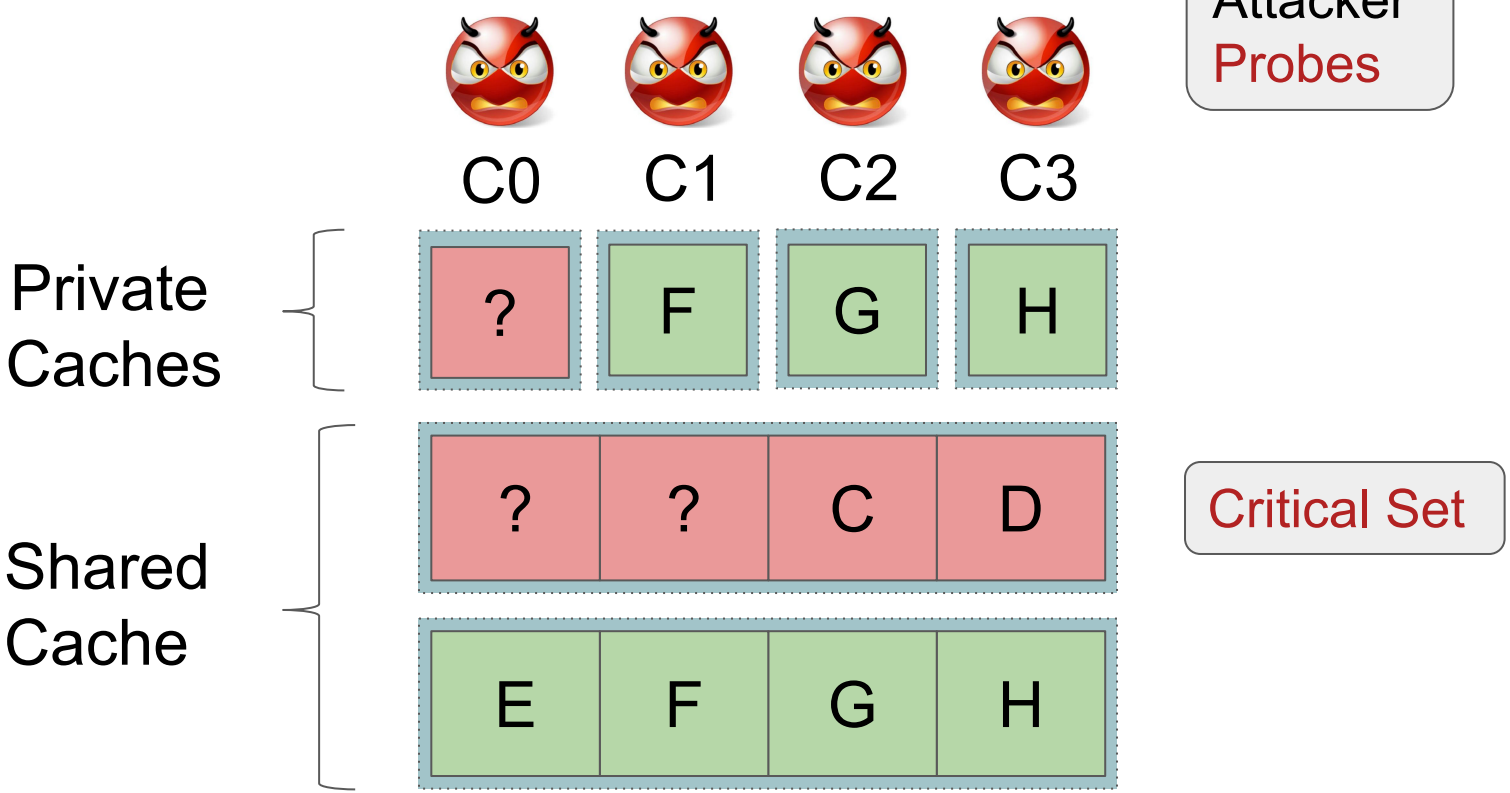

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No ☹

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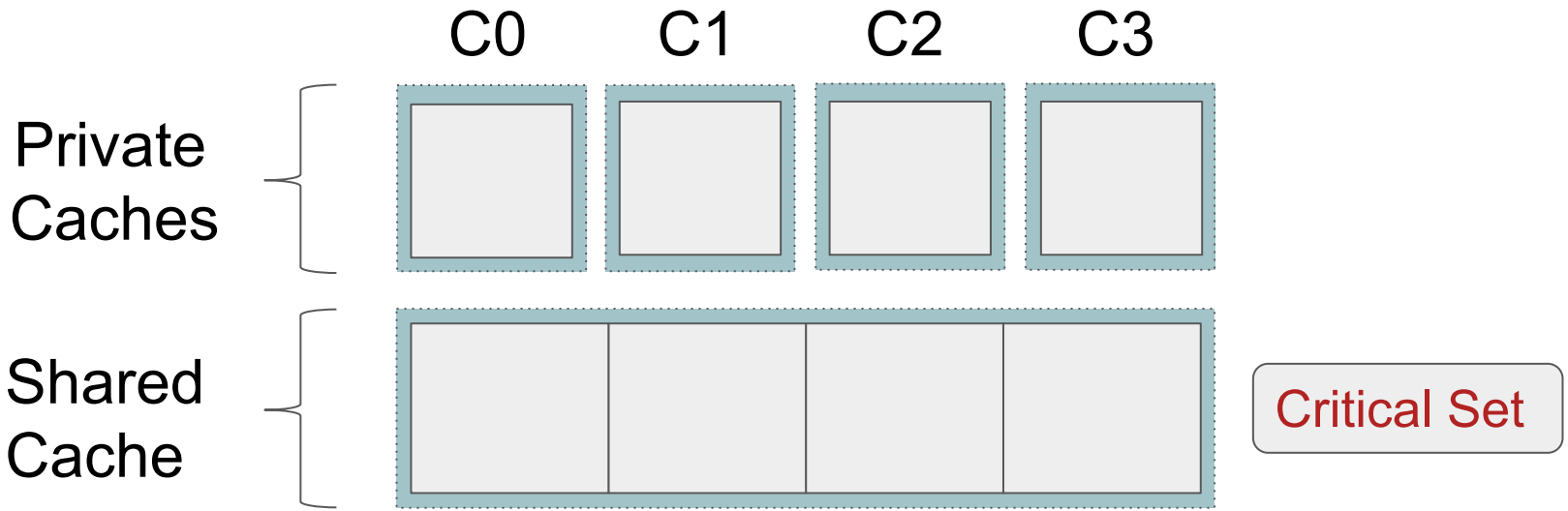
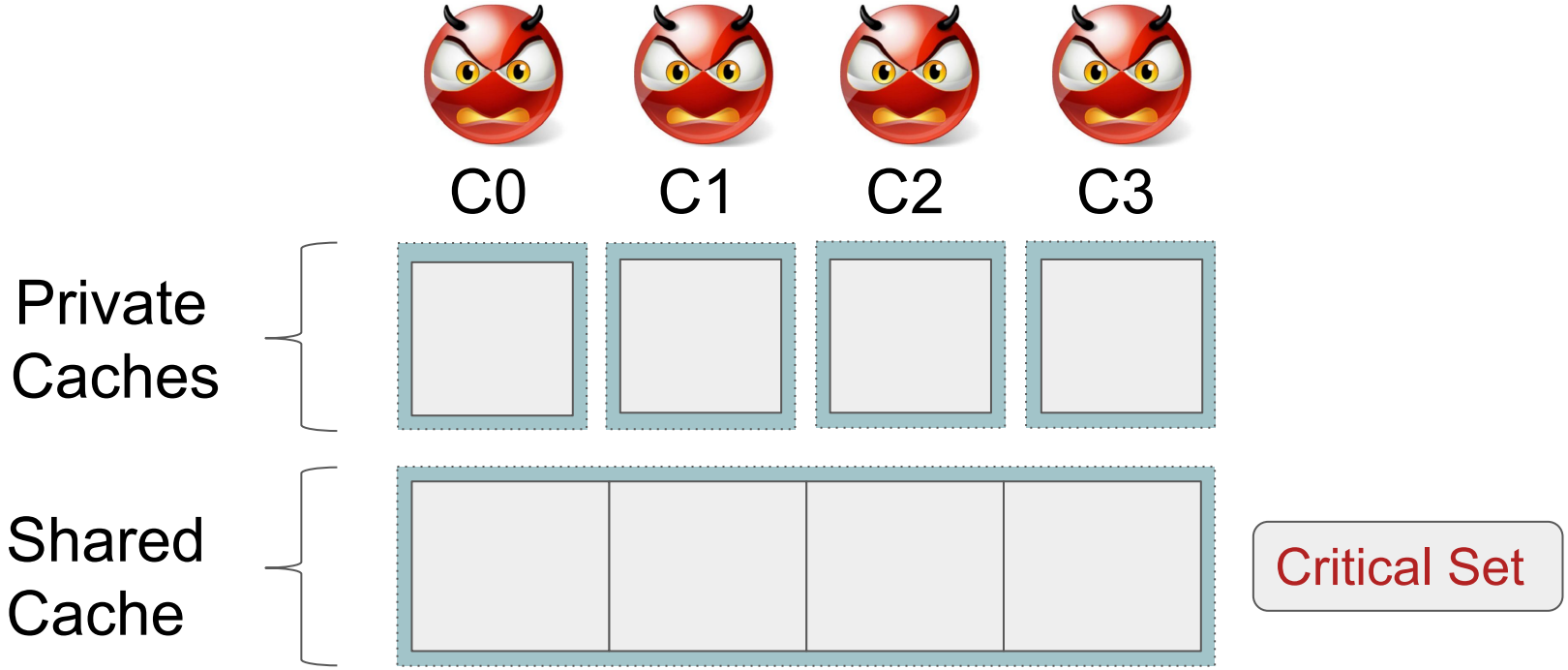
Denial of Service Attack



Denial of Service Attack

Multi-threaded Attacker



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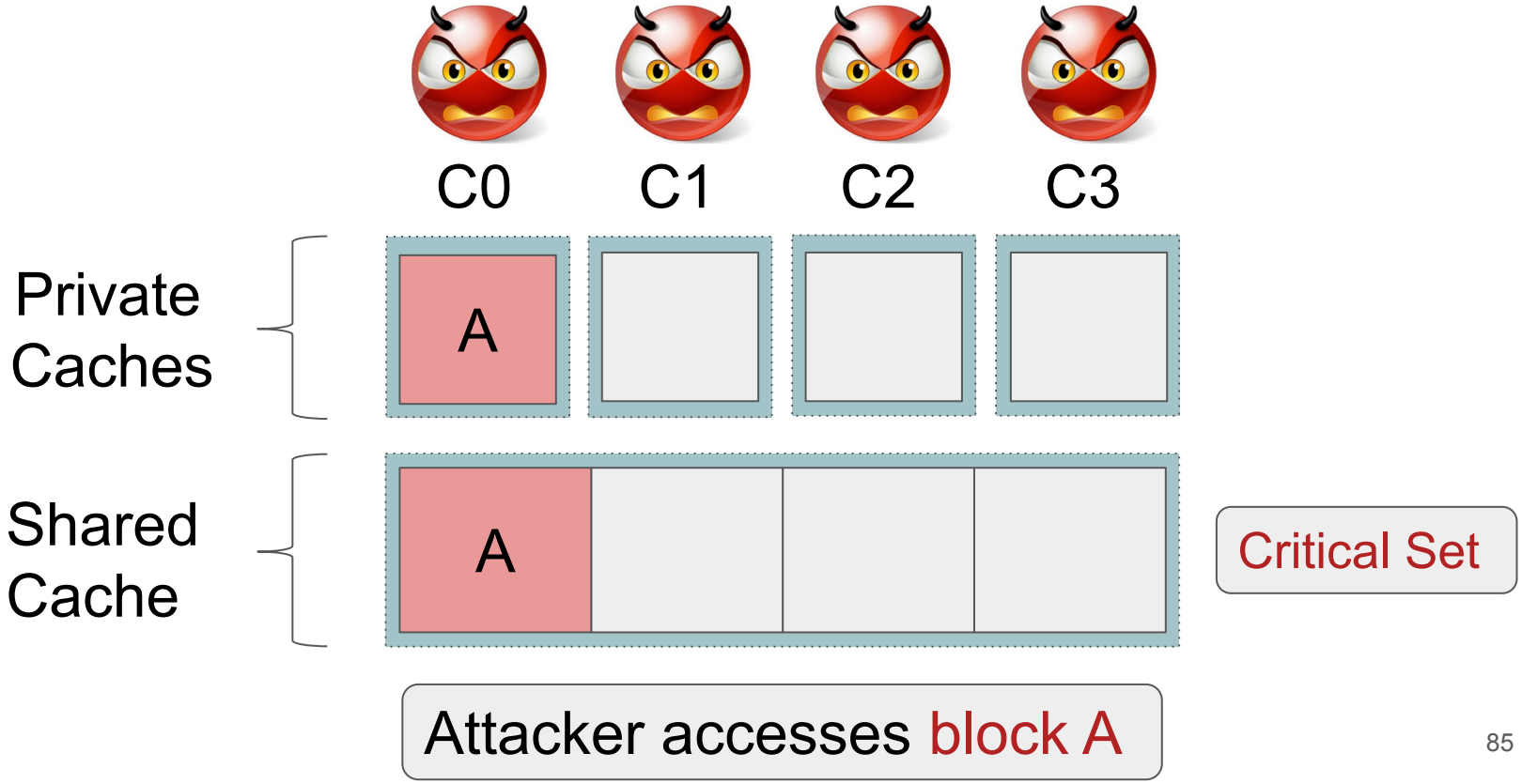
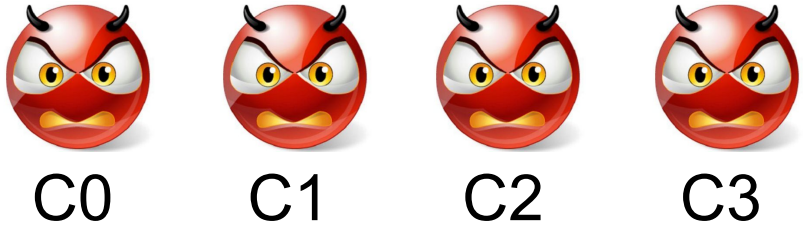
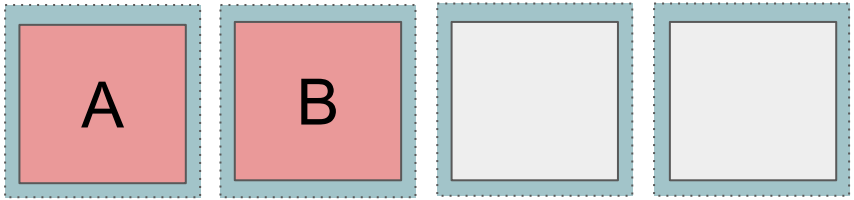


Denial of Service Attack

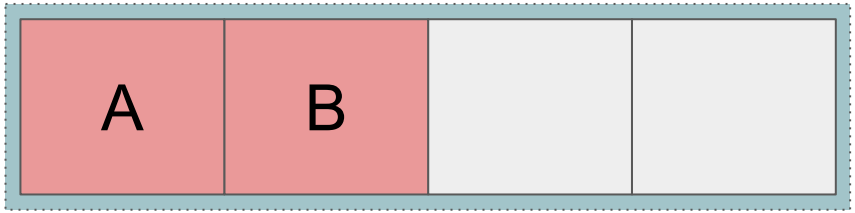


C0 C1 C2 C3

Private Caches



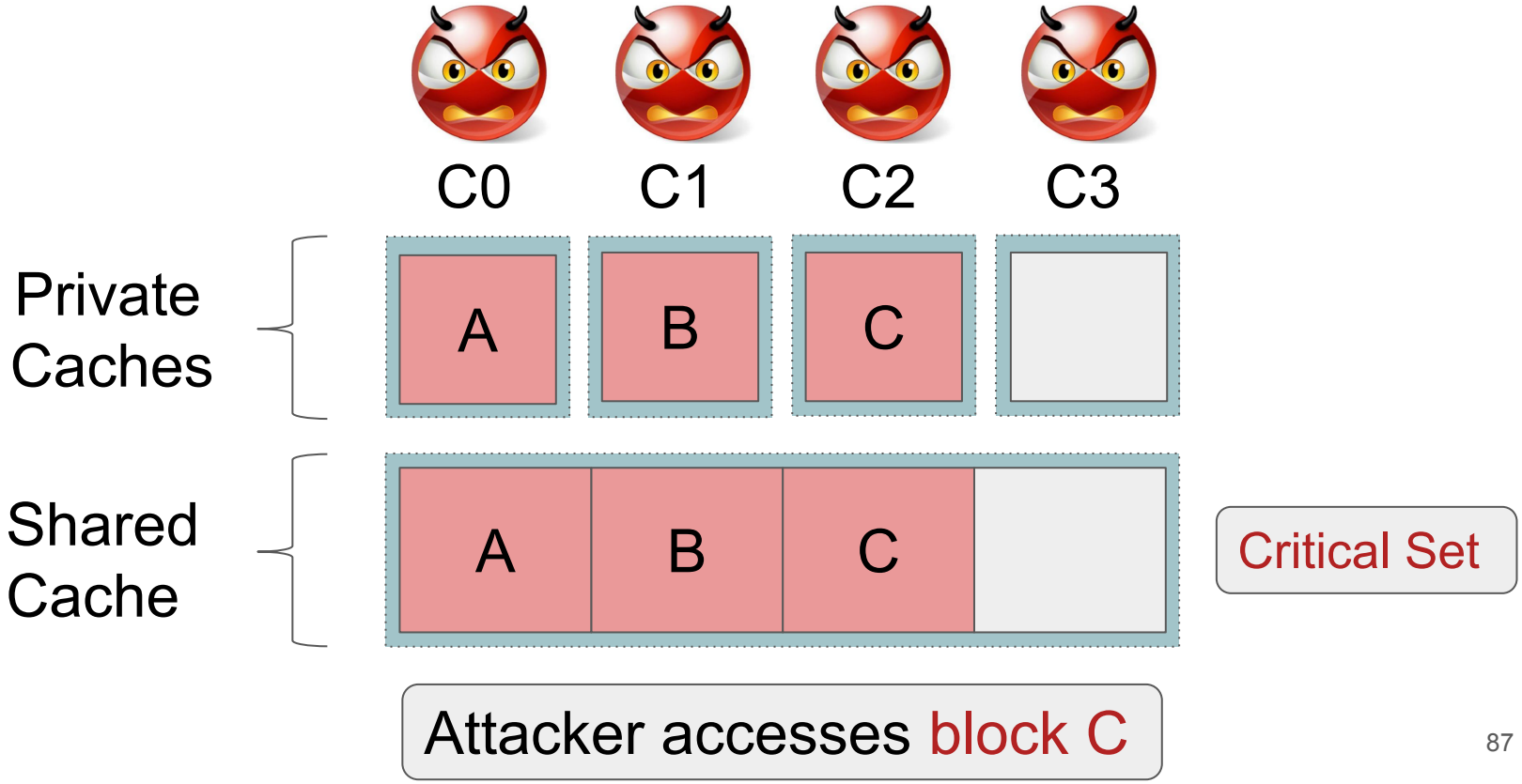
Shared Cache



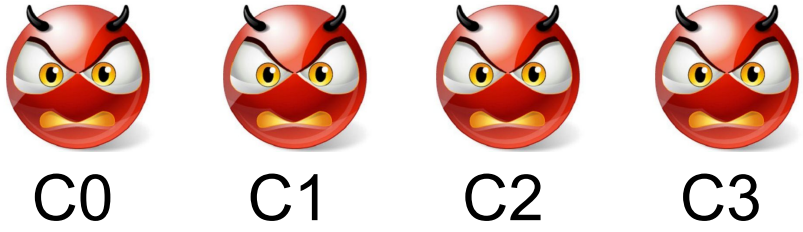
Critical Set

Attacker accesses block B

Denial of Service Attack



Denial of Service Attack



C0 C1 C2 C3

Private Caches

A B C D

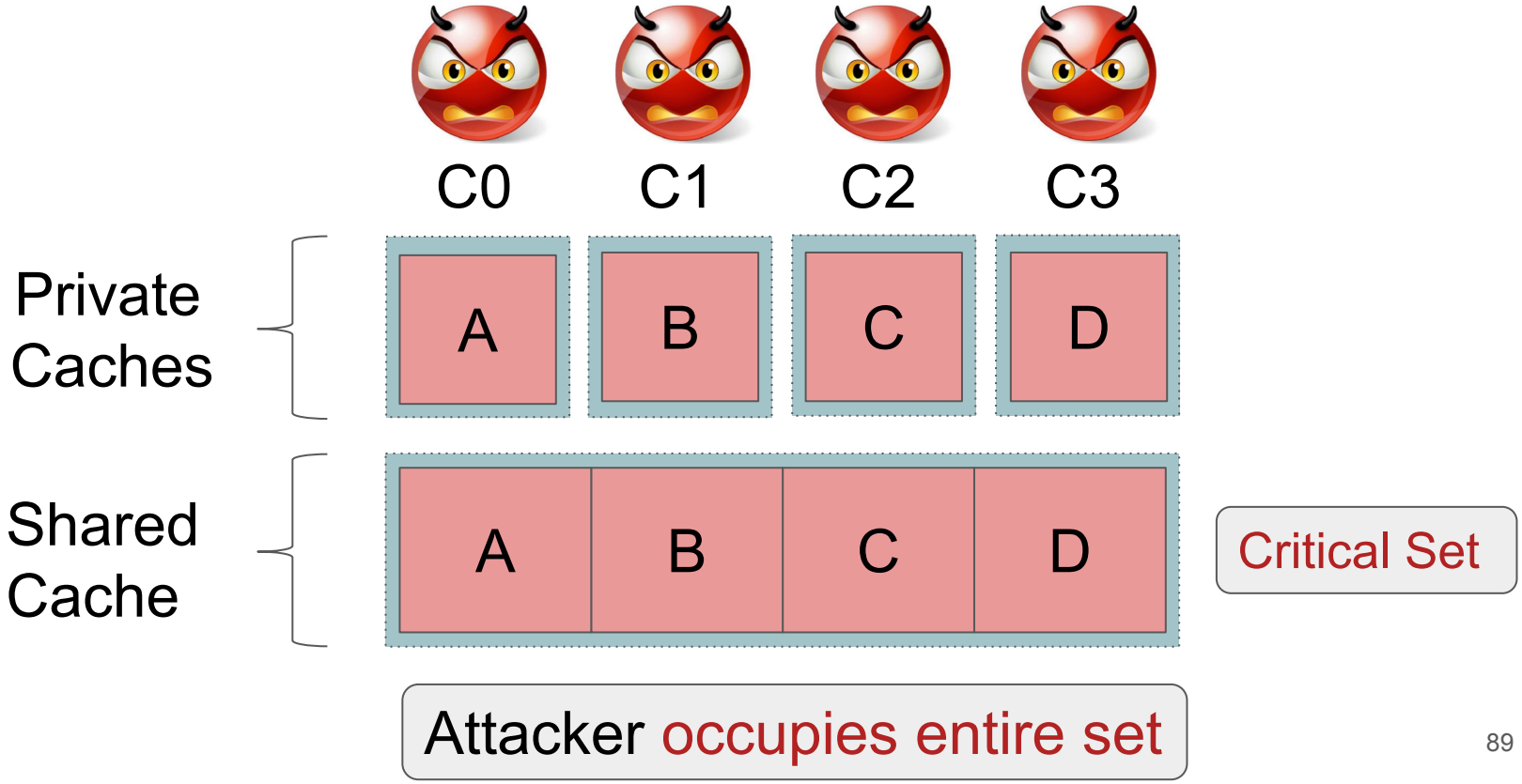
Shared Cache

A B C D

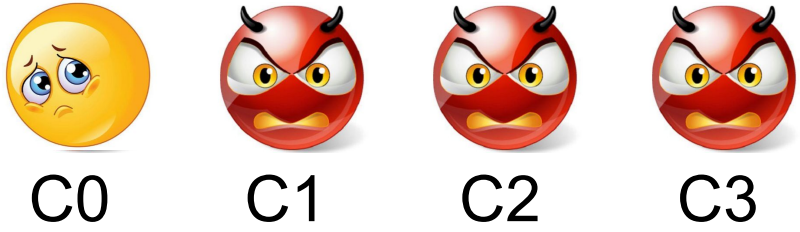
Critical Set

Attacker accesses block D

Denial of Service Attack



Denial of Service Attack



C0 C1 C2 C3

Private Caches

A B C D

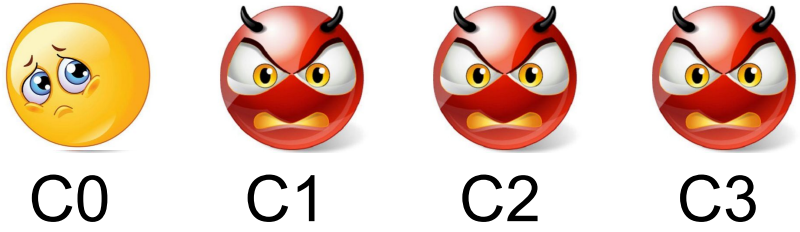
Shared Cache

A B C D

Critical Set

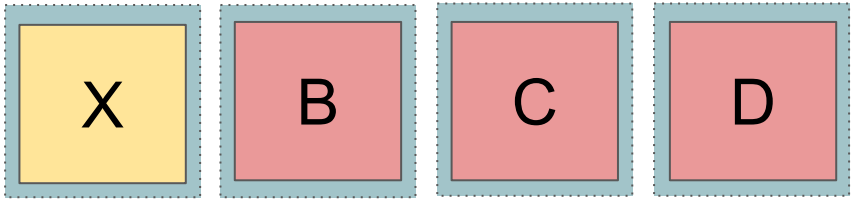
Victim comes

Denial of Service Attack

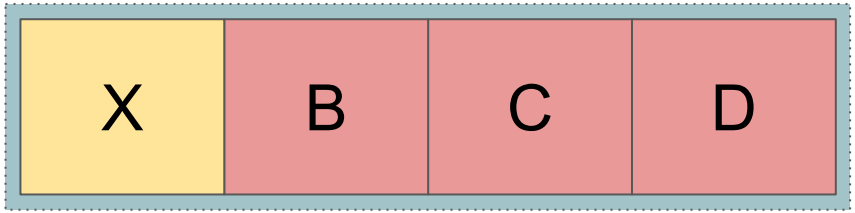


C0 C1 C2 C3

Private Caches



Shared Cache



Critical Set

Victim accesses block X

Denial of Service Attack

C0 C1 C2 C3

Private Caches

Y B C D

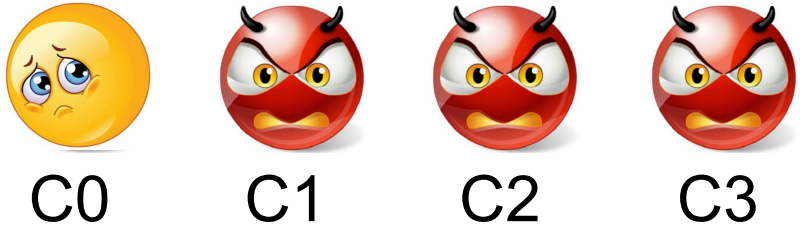
Shared Cache

Y B C D

Critical Set

Victim accesses block Y

Denial of Service Attack



C0 C1 C2 C3

Private Caches

Z B C D

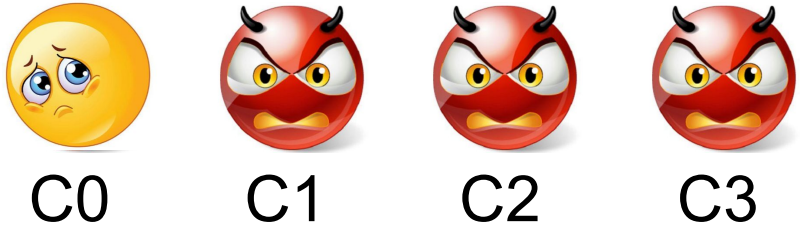
Shared Cache

Z B C D

Critical Set

Victim accesses block Z

Denial of Service Attack



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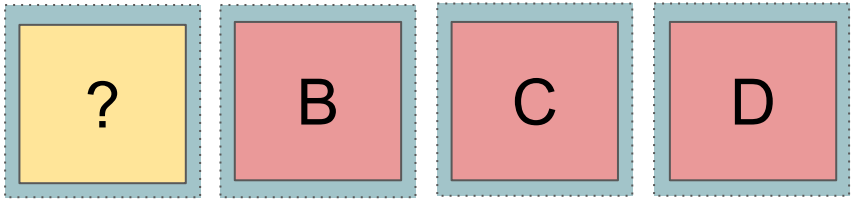
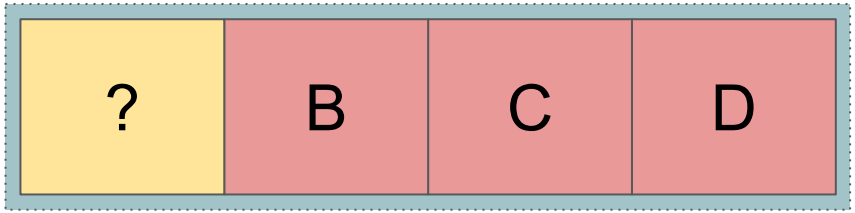
Shared Cache





Critical Set

Victim strives for other ways

Questions That We Ask?

Does SHARP mitigate all attacks?

No ☹

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Yes ☹

Questions That We Ask?

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Does threshold affect benign applications?

Simulation

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ChampSim, a trace driven simulator

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Simulated SHARP on a 16-core system with three levels of caches and huge pages

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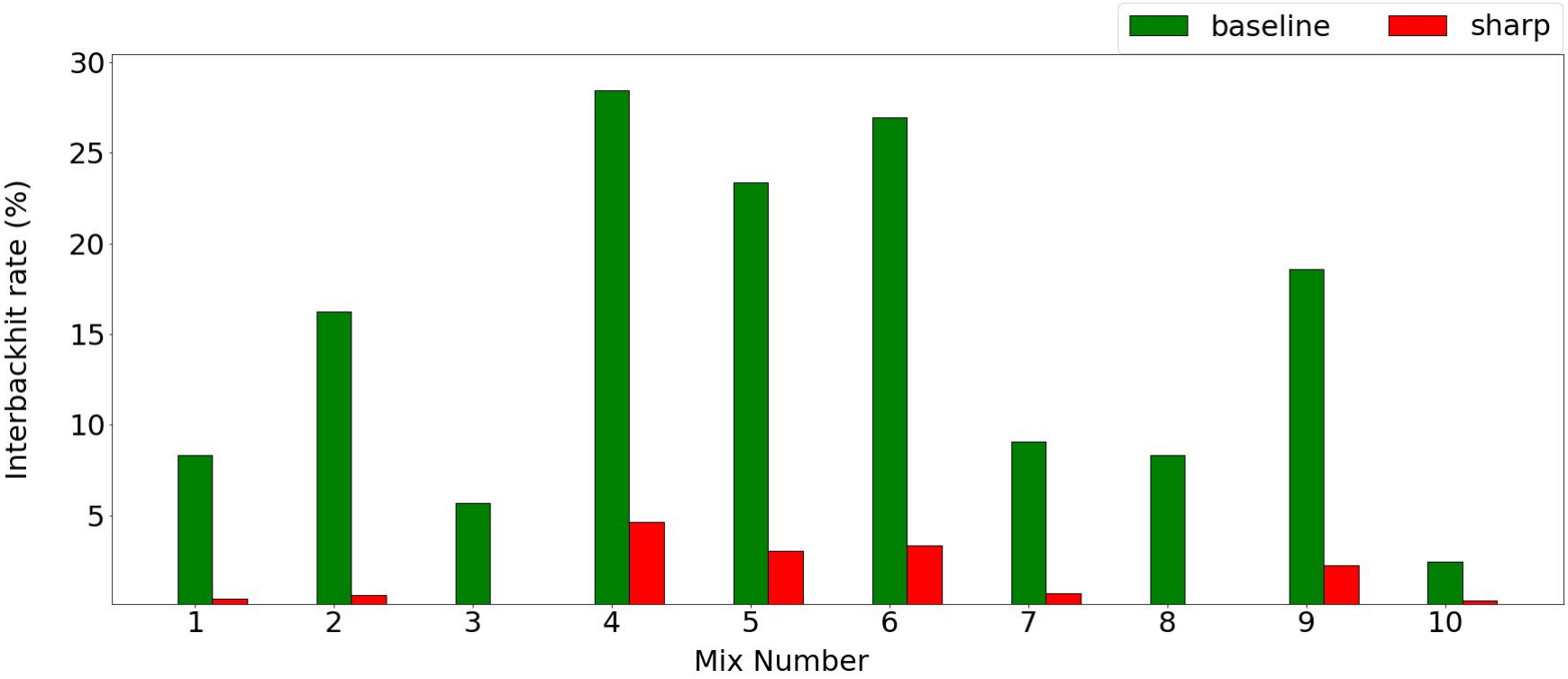
Used different combinations of LLC thrashing and LLC fitting applications
Example, 16:0 denotes 16 thrashing and zero fitting

LLC Thrashing Benchmarks [SPEC CPU 2017]

Mix No	Thrashing Benchmarks
1	605.mcf-484B
2	605.mcf-665B
3	605.mcf-994B
4	607.cactubssn-2421B
5	620.omnetpp-141B
6	620.omnetpp-874B
7	621.wrf-6673B
8	623.xalancbmk-10B
9	649.fotonik-10881B
10	654.roms-523B

Interbackhit Rate



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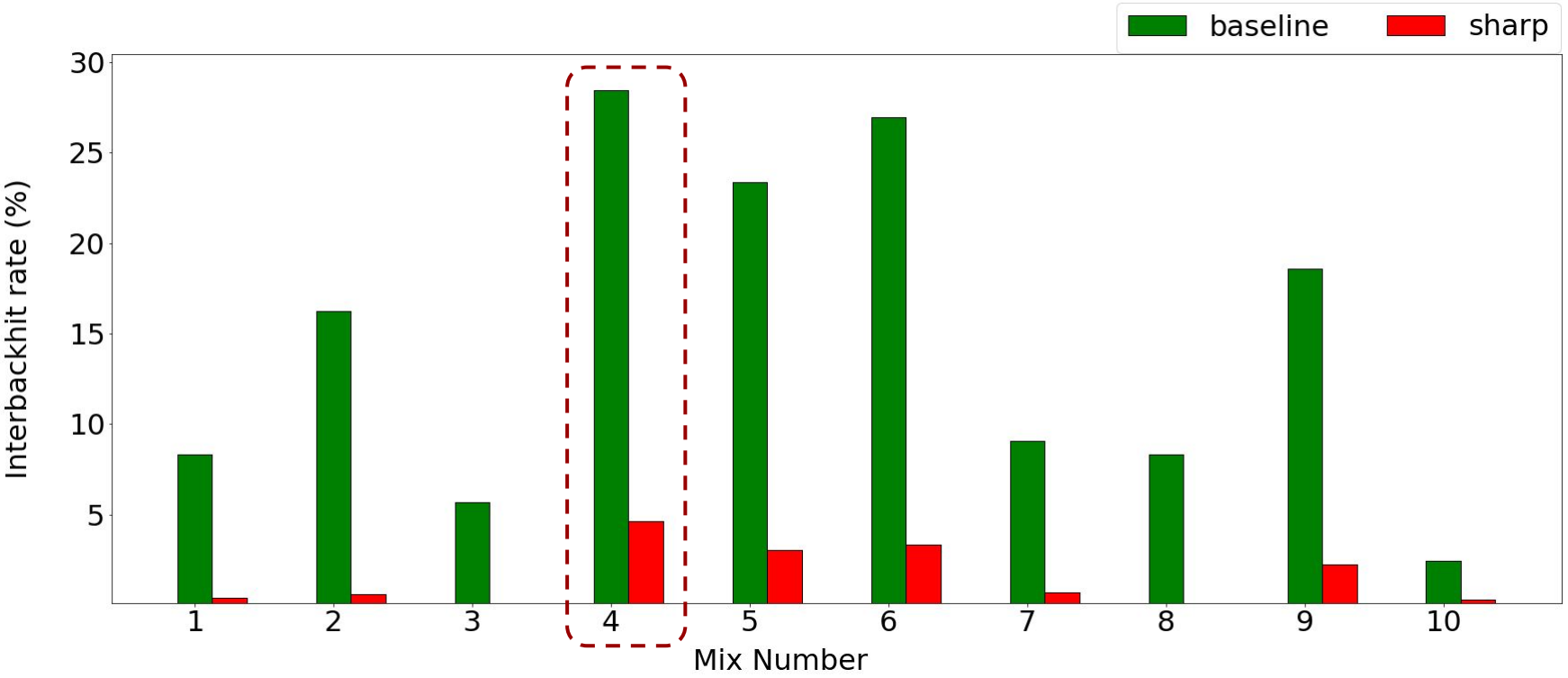
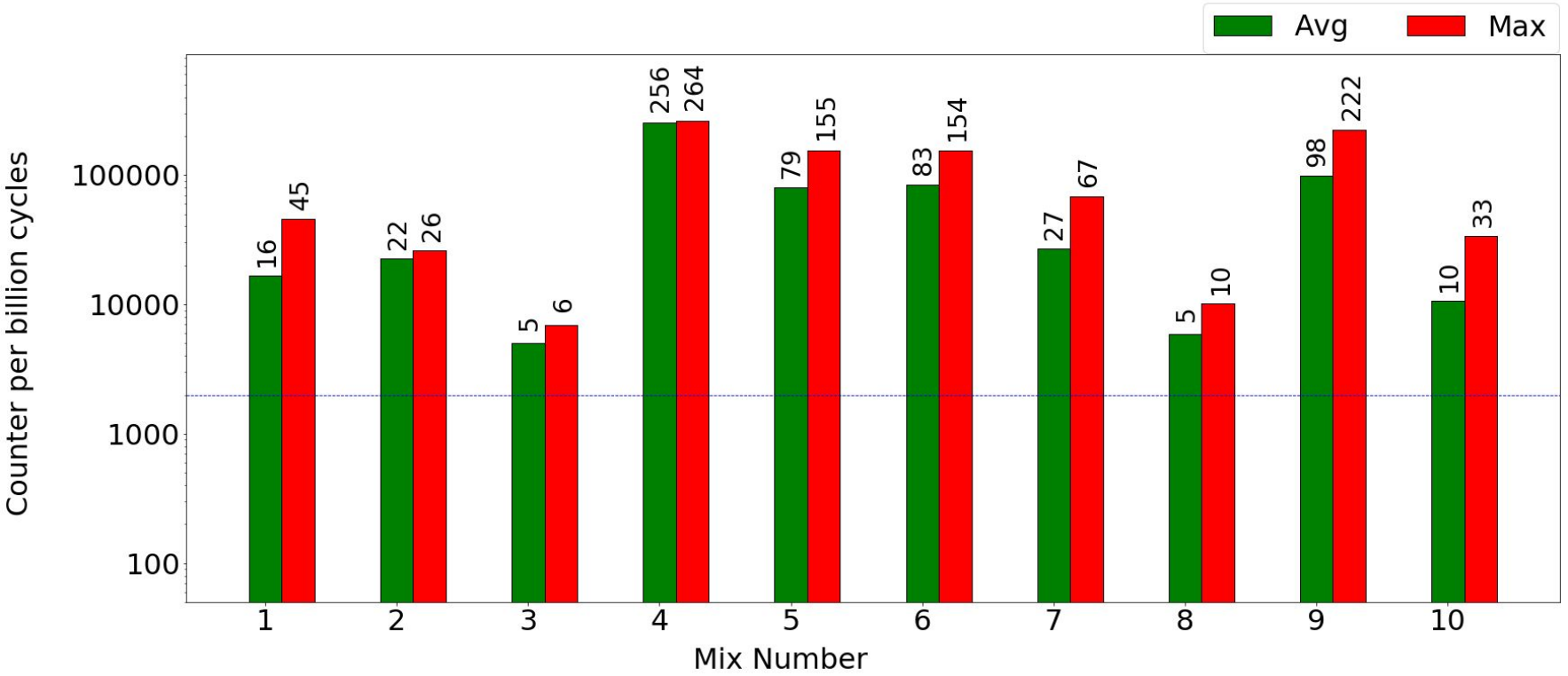


Interbackhit Counter



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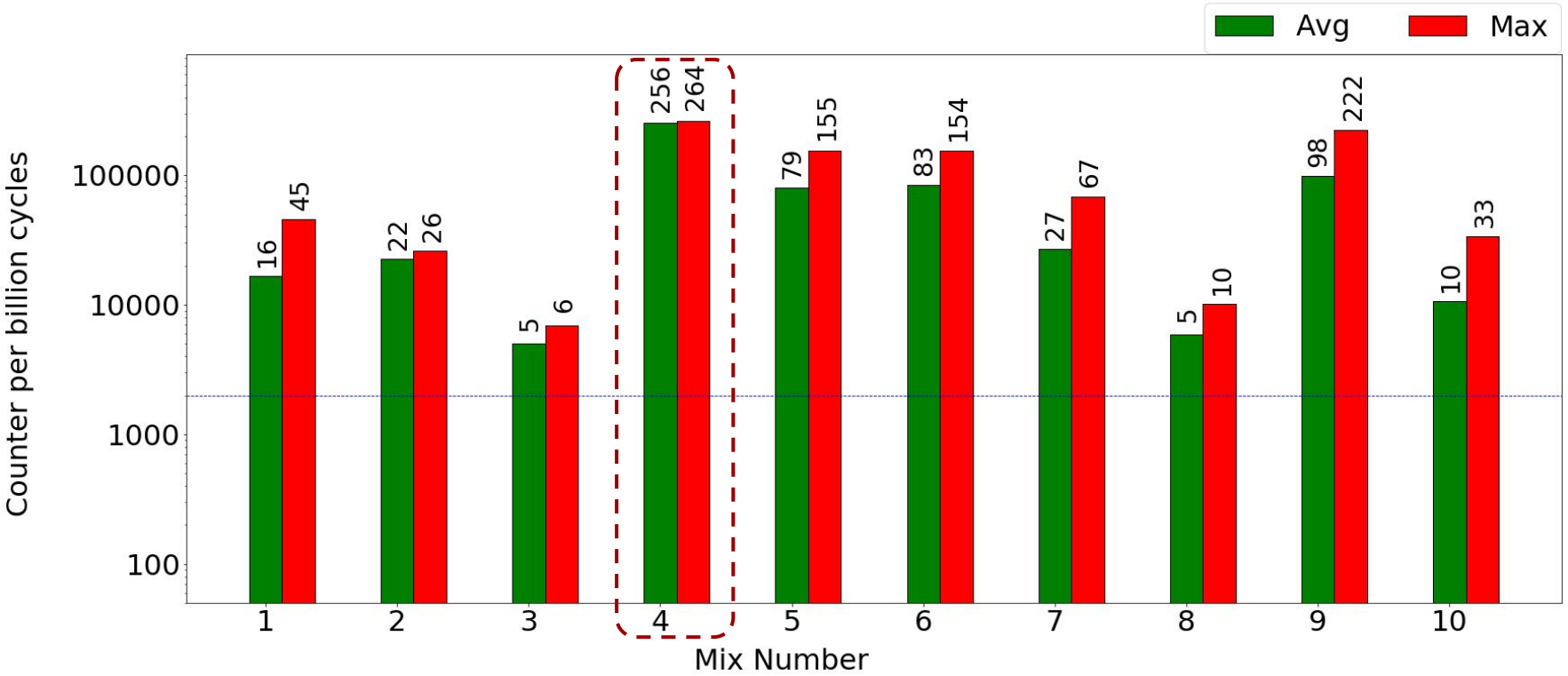

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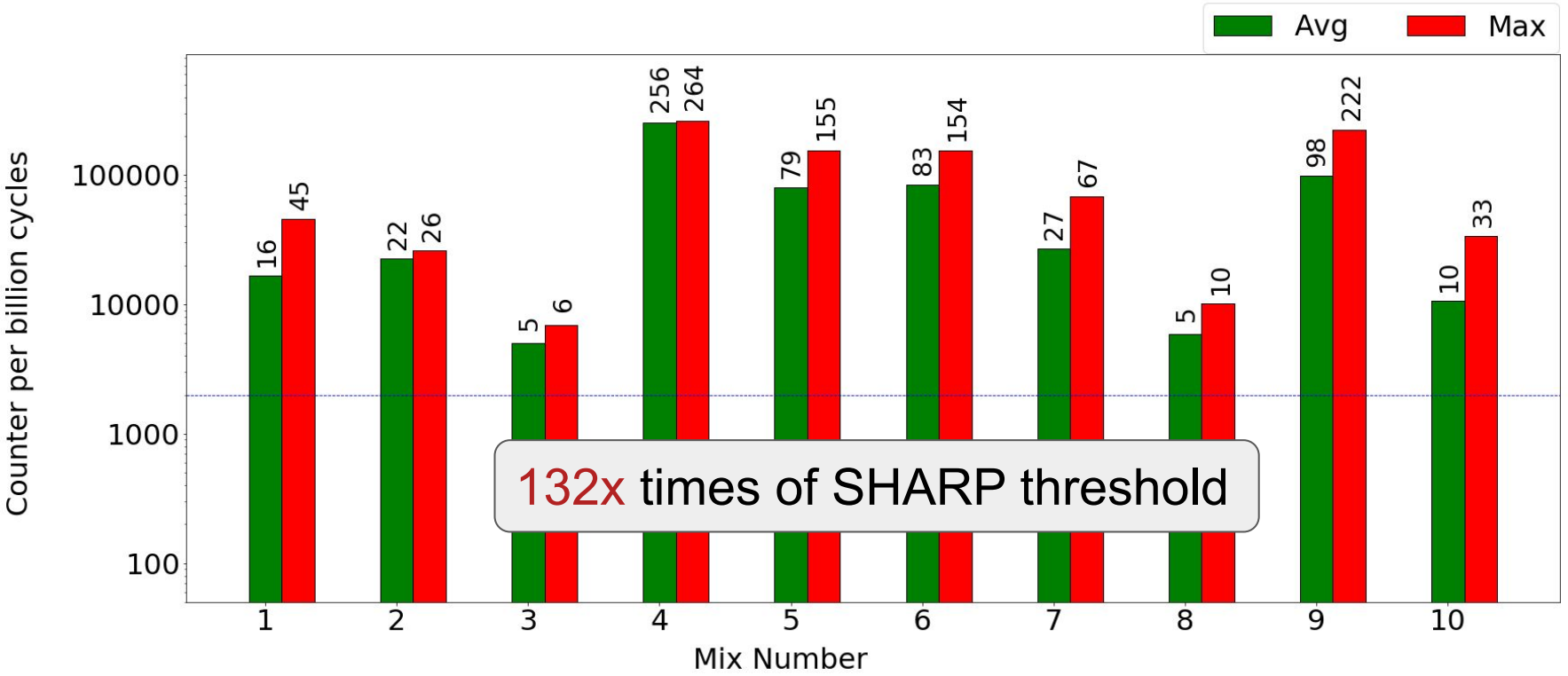

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What does OS do when it receives an interrupt?

Speculating Possible OS Mitigations

Speculating Possible OS Mitigations

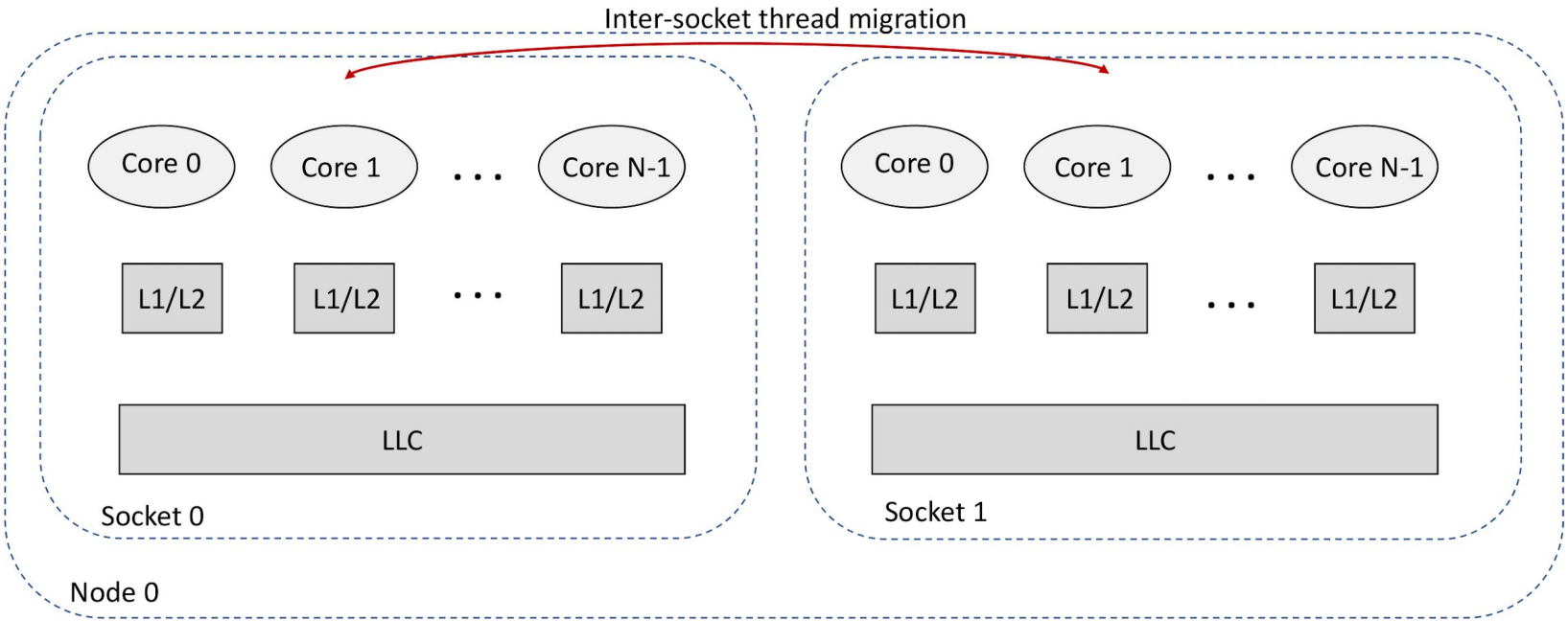
To deschedule

Speculating Possible OS Mitigations

To deschedule

To migrate to another socket

Migration to Another Socket



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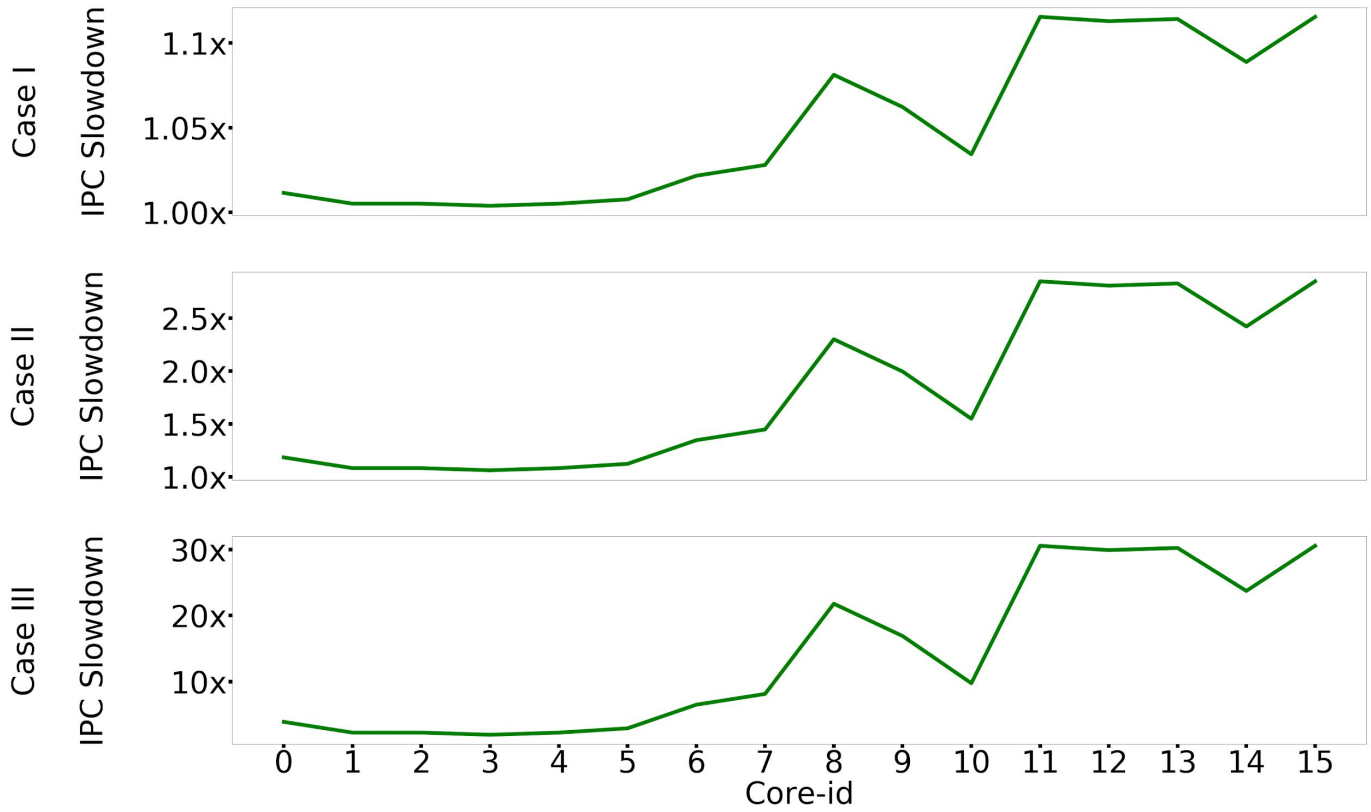
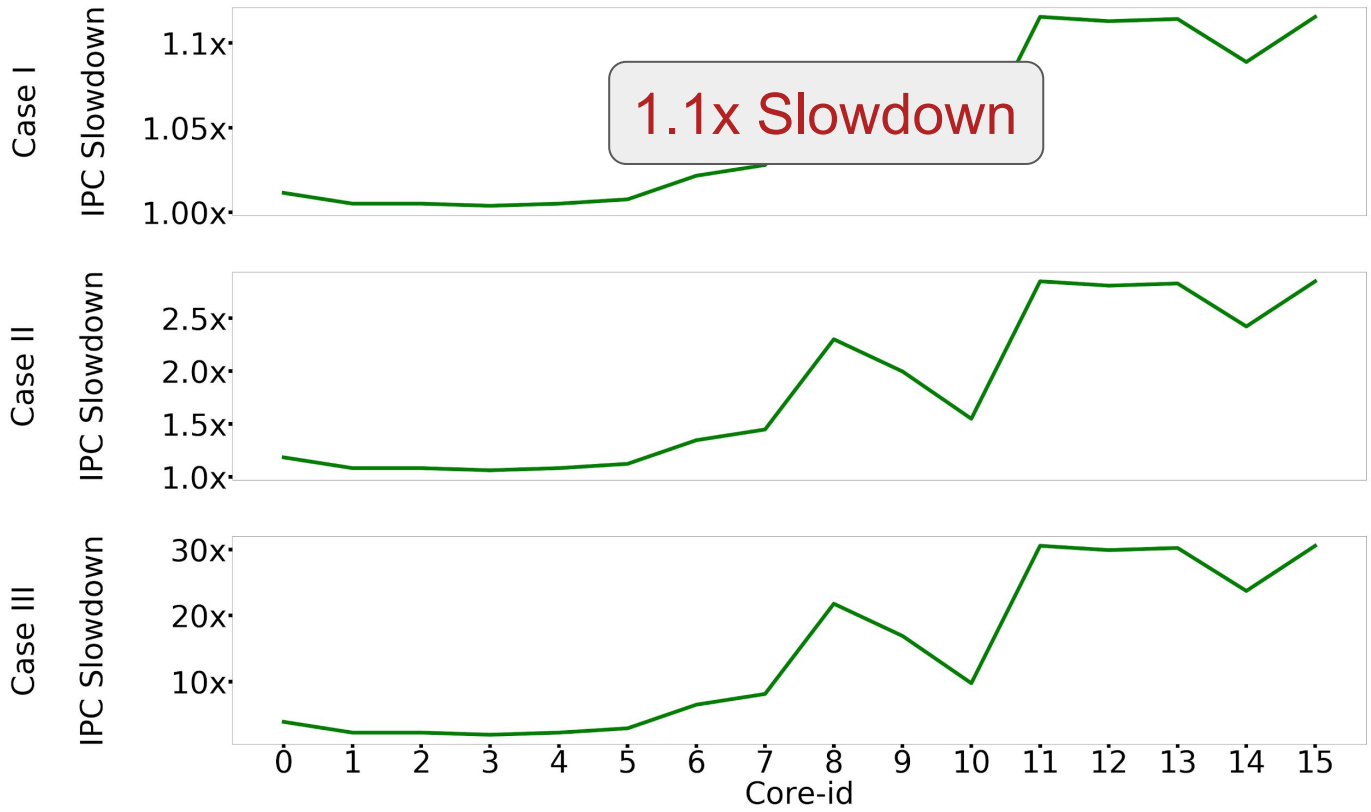
Causes performance overhead

Delay Cost : IPC Slowdown



Case	Mitigation Delay
I	1 Million cycle
II	16 Million cycle
III	256 Million cycle

Delay Cost : IPC Slowdown



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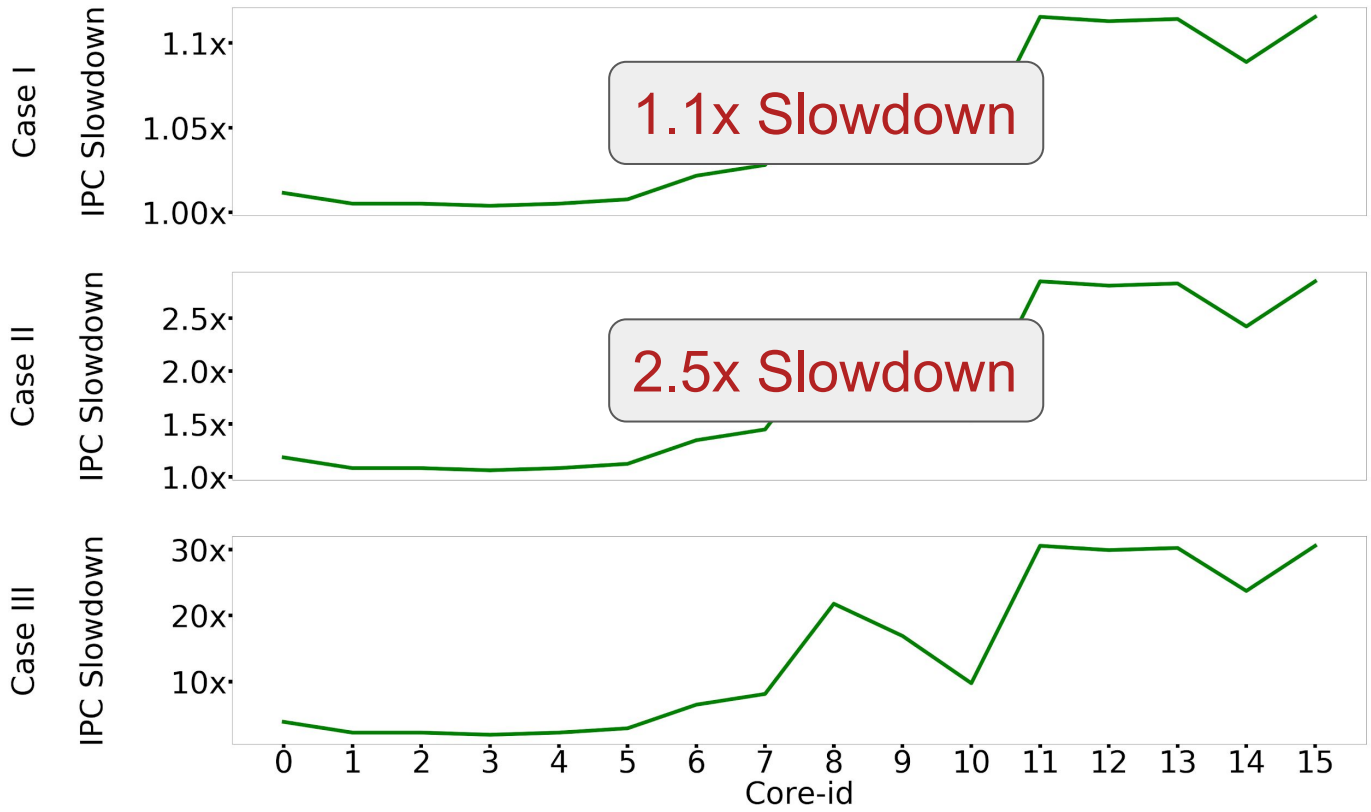

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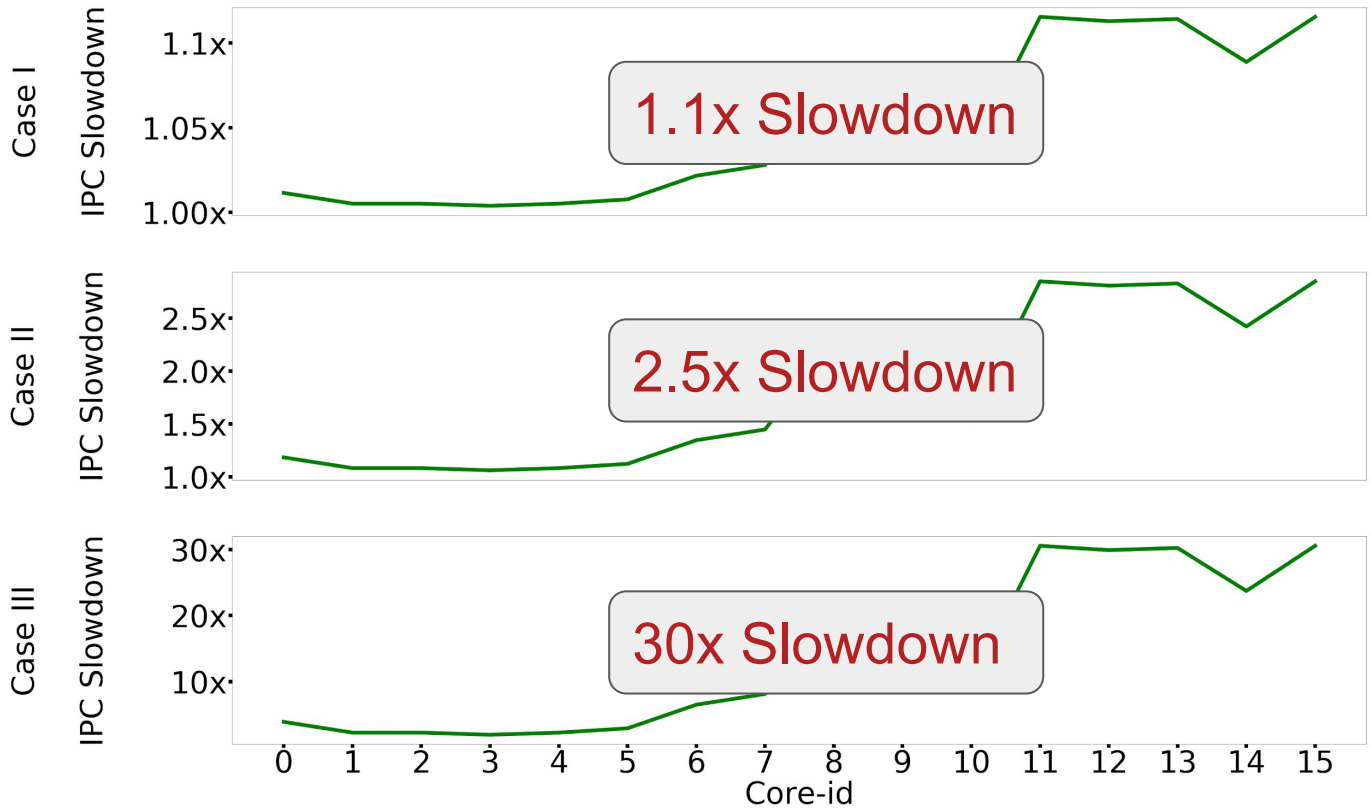

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16-0 Mix, 100% apps got killed ☹

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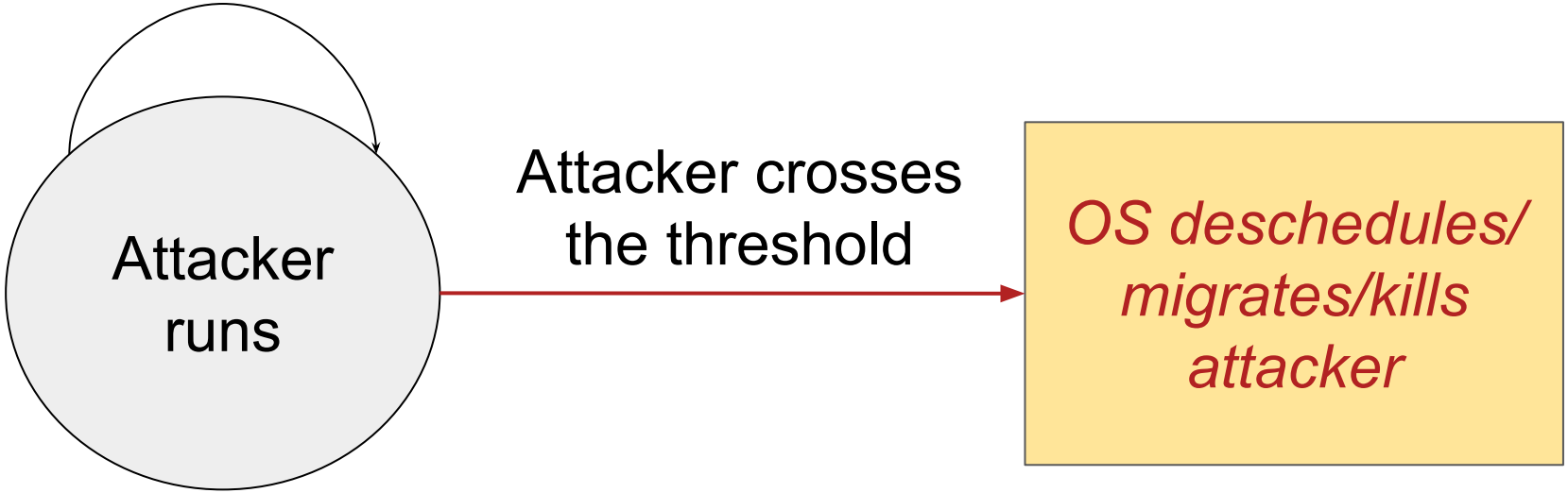
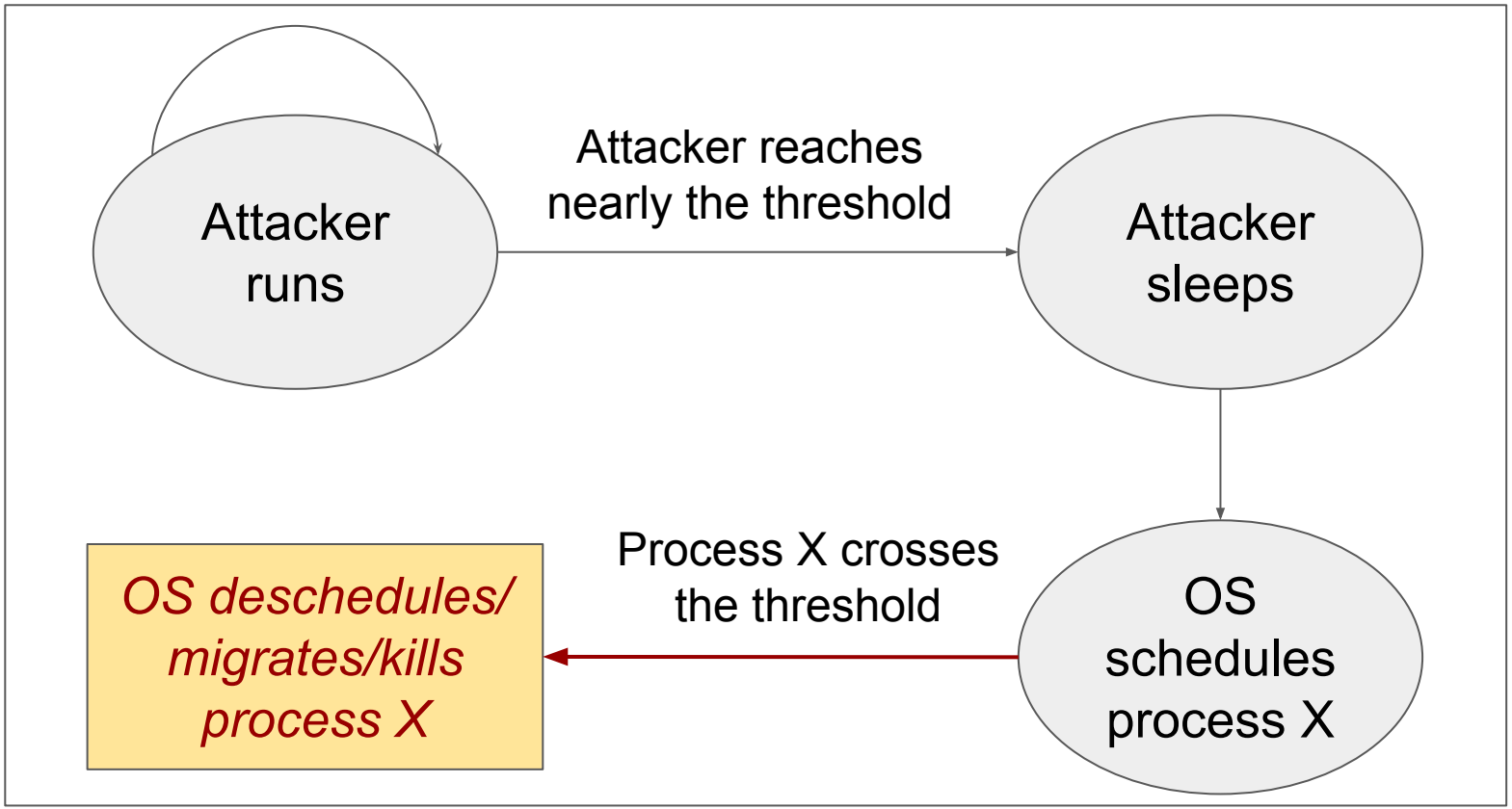
Does mitigation strategy facilitates any new attack?

Threshold Aware Attack - I



Threshold Aware Attack - II



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Is SHARP secure in terms of information leakage?

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What does OS do when it receives an interrupt?

Is SHARP secure in terms of information leakage? — *Not really* ☹

Conclusion

SHARP is not that sharp

Facilitates new attacks

Don’t mitigates all attacks

Role of OS is not defined

Performance overhead to benign applications

Thank You!

Semiconductor Research Corporation