FAST'21

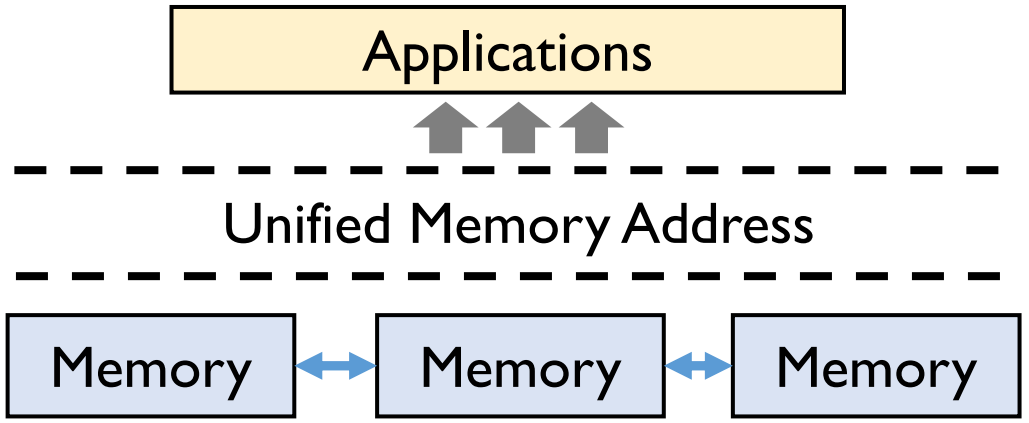
Concordia: Distributed Shared Memory with In-Network Cache Coherence

Qing Wang, Youyou Lu, Erci Xu, Junru Li, Youmin Chen, Jiwu Shu

Tsinghua University

Distributed Shared Memory (DSM)

- **Classic DSM (early 1990s)**
  - Unified memory space
  - Ease programming for distributed apps



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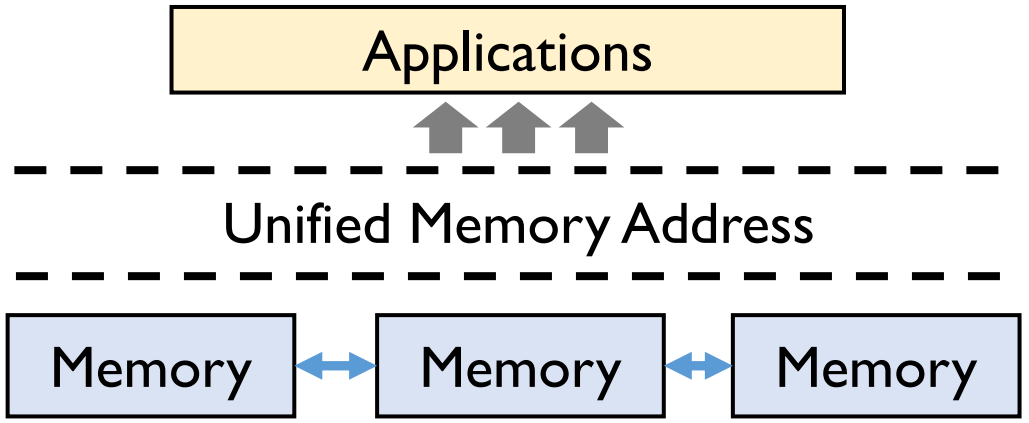

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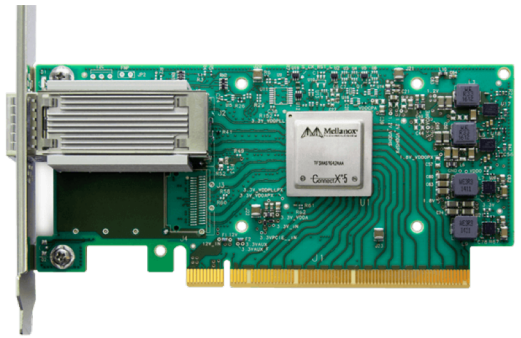
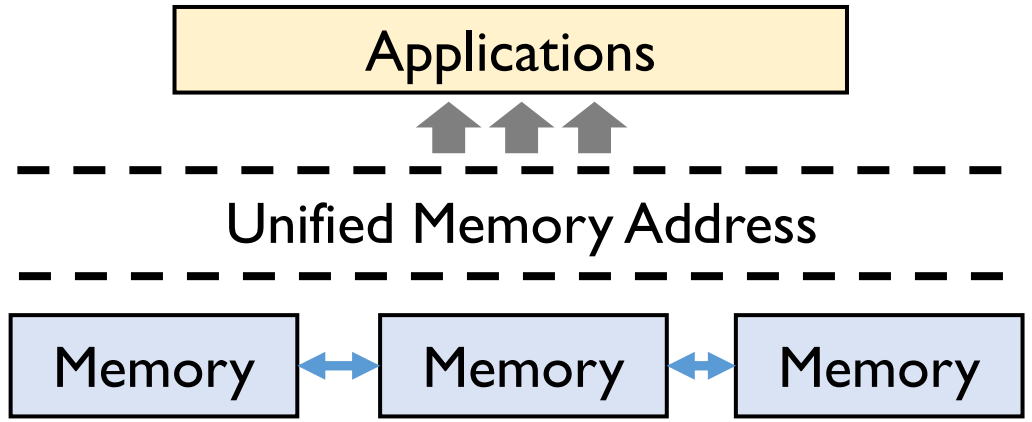
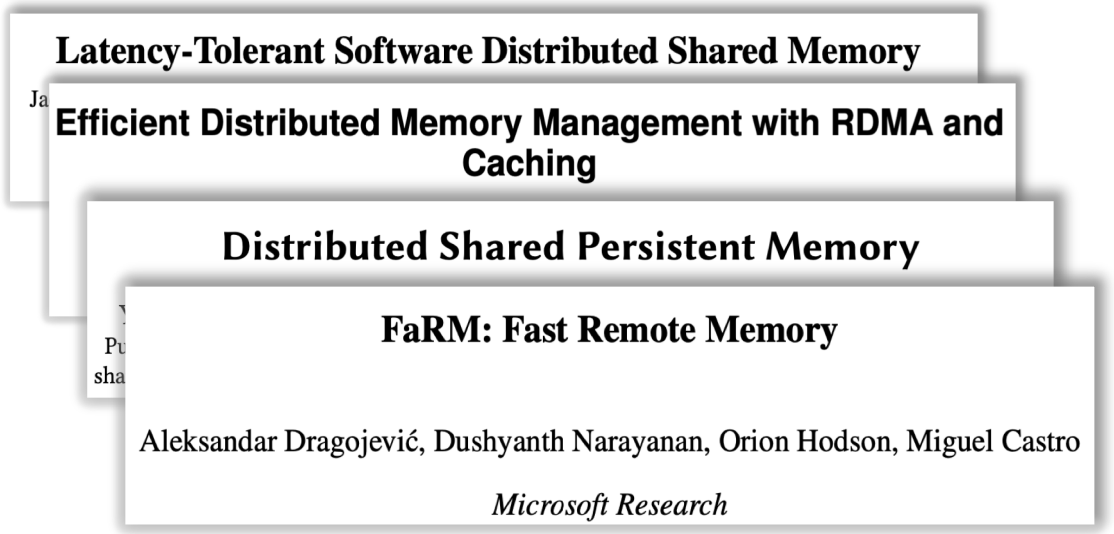
  - Unified memory space
  - Ease programming for distributed apps
  - Failed due to unsatisfying performance
- **Modern DSM (2010 - now)**
  - Sparked by fast network (e.g., RDMA)
  - Support modern apps (e.g., OLTP, Graph)
  - Example: Microsoft's FaRM



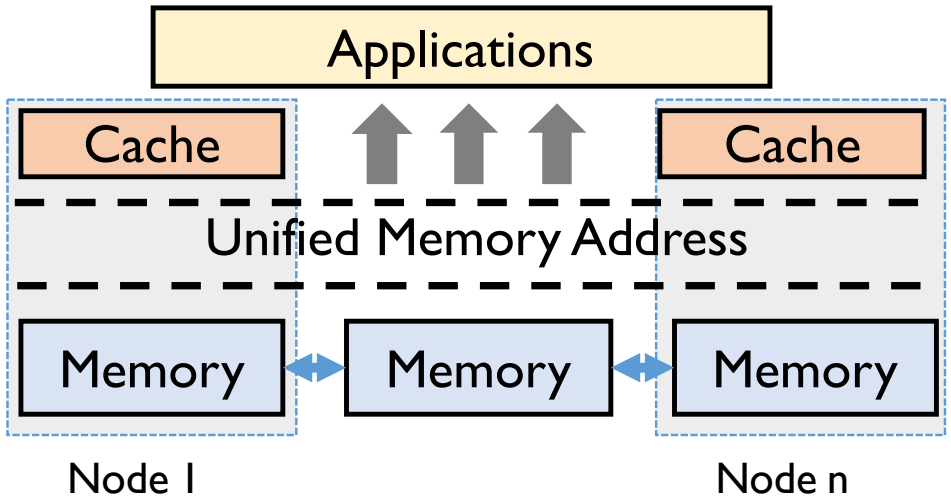
Mellanox Connectx-5
100Gbps, RTT < 2µs





Caching & Coherence

- **Still, caching is a must**
  - Boost performance
  - Bandwidth: local mem vs. network → 2-4X
  - Latency: local mem vs. network → 12X



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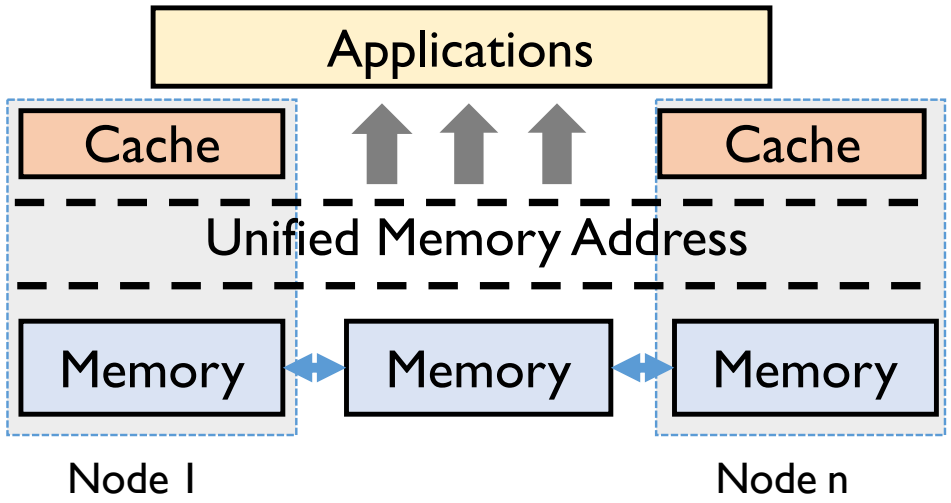

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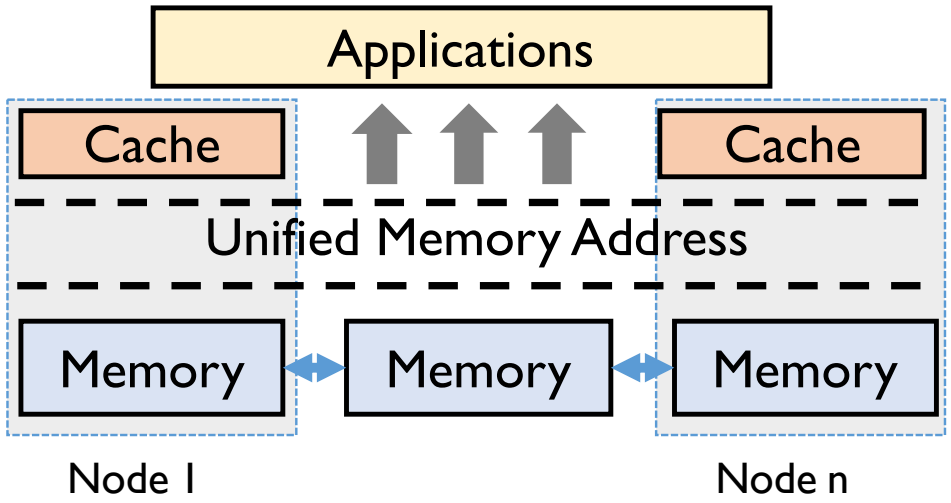

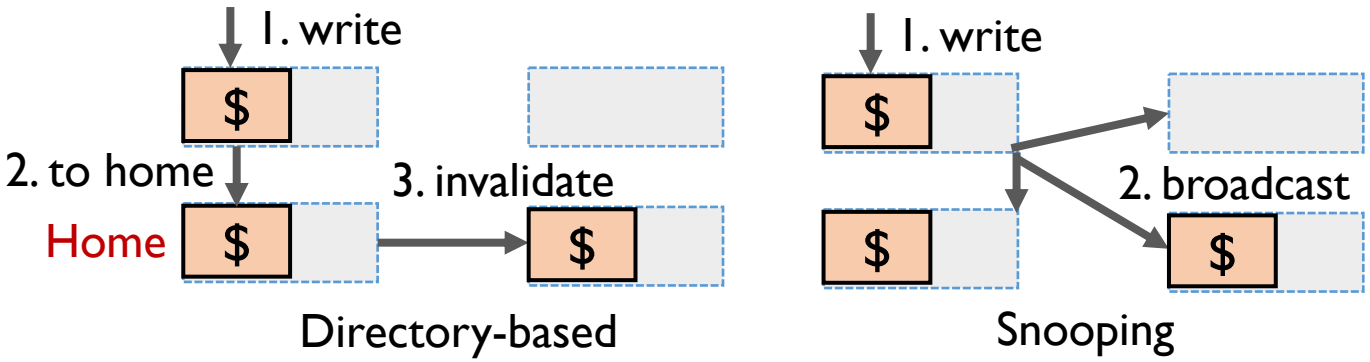

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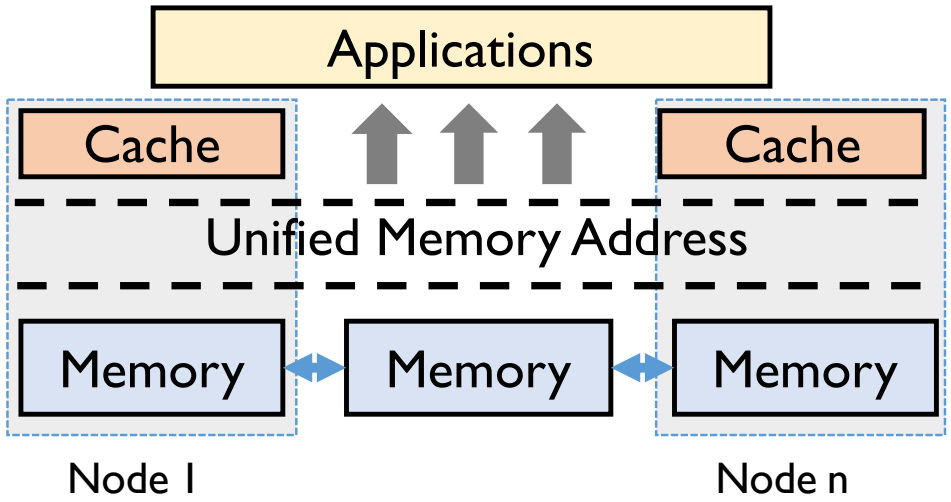
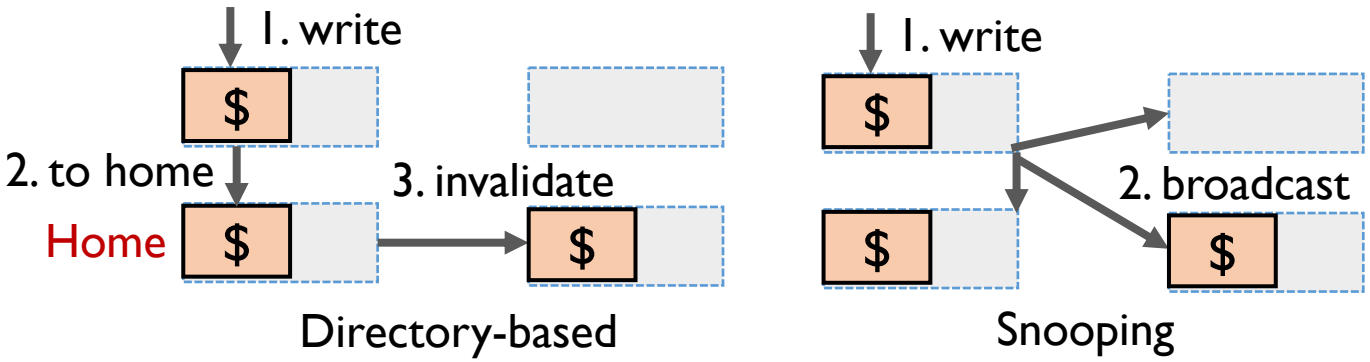
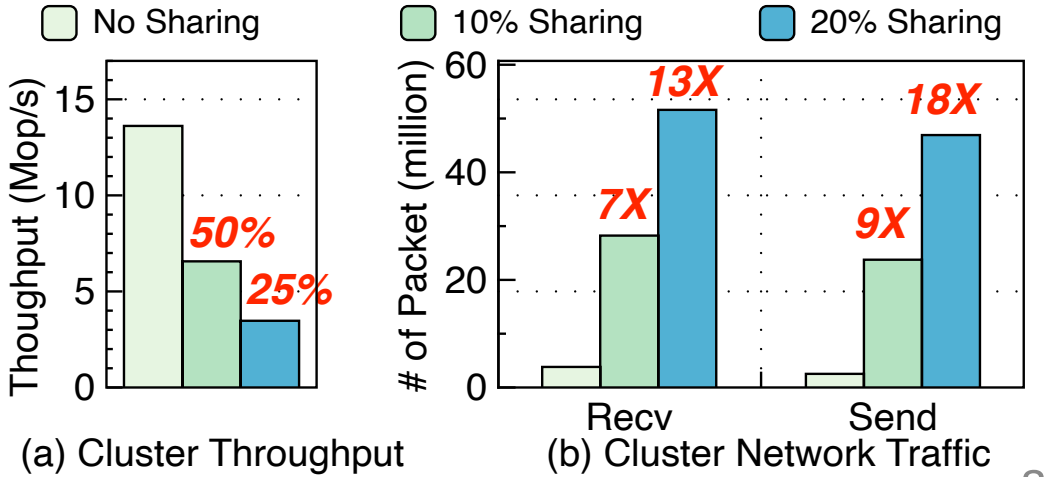


GAM [VLDB'18], directory coherence using RDMA





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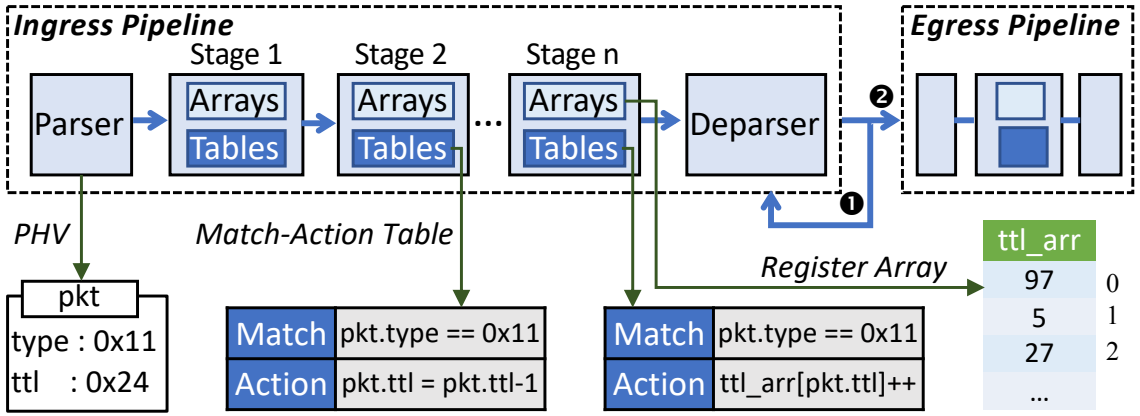
Opportunities from Programmable Switches

BAREFOOT NETWORKS | an Intel company

BROADCOM® connecting everything®

user-defined line-rate network protocols



match-action pipeline

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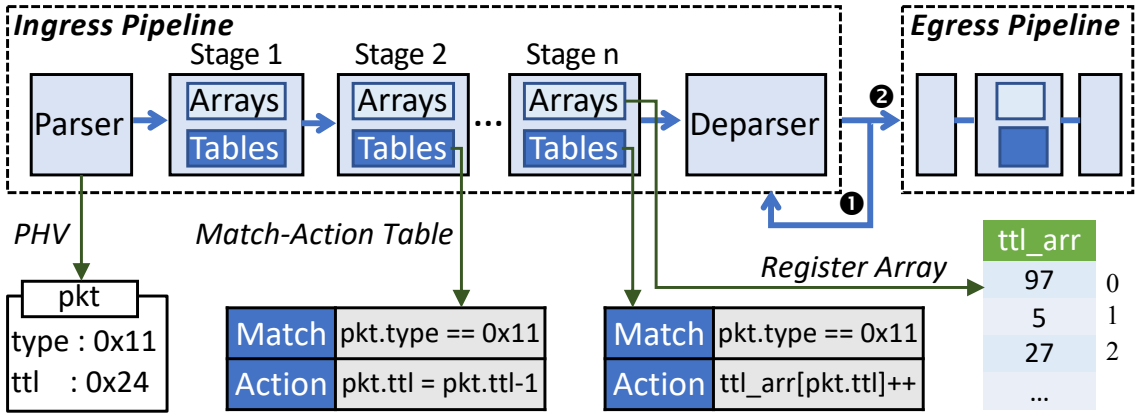

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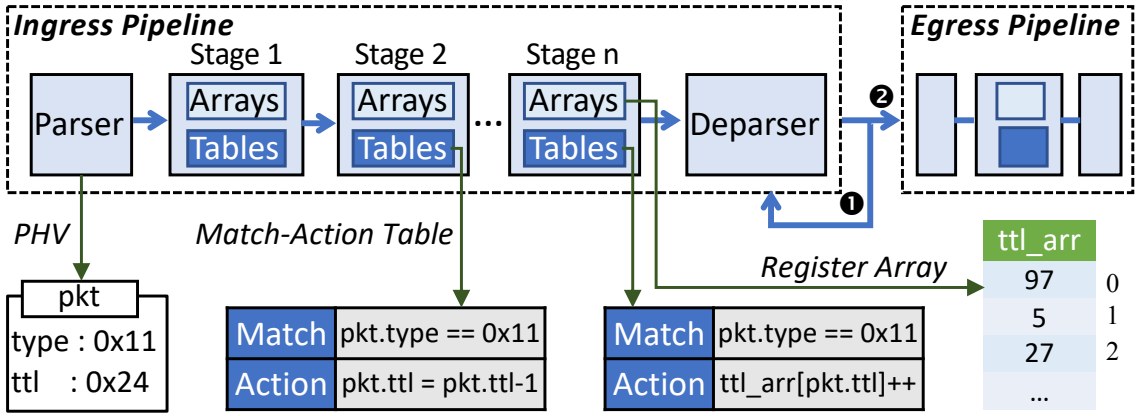

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- Centralized hub & line-rate forwarding

Coherence Protocols

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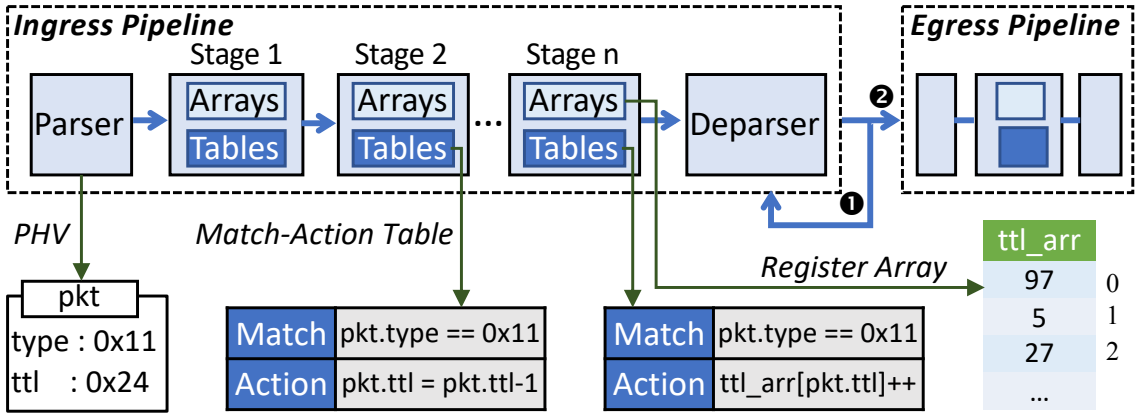

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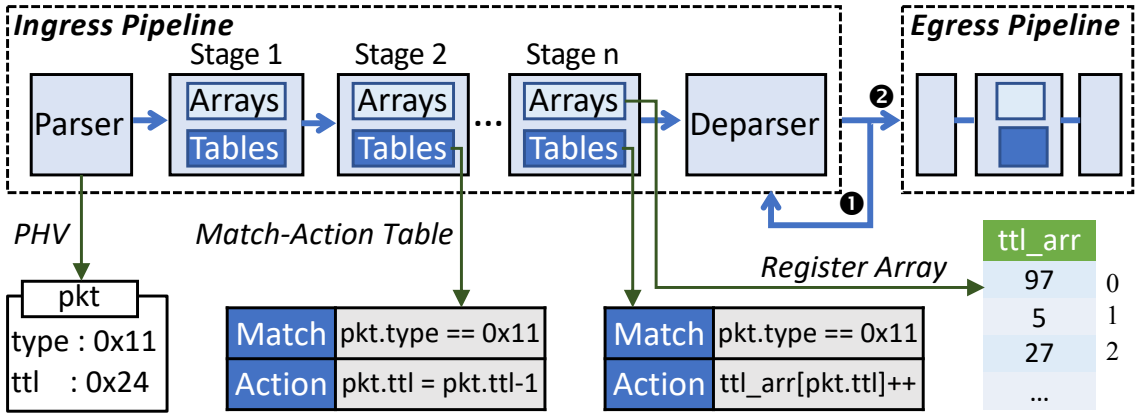

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Using programmable switches to handle cache coherence is promising …

Programmable Switches

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- On-chip memory (i.e., register arrays)
- Atomic read-modify-write

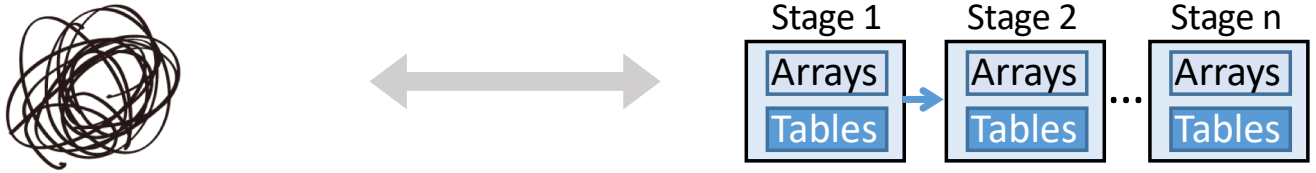
Coherence Protocols

- Multicast invalidation
- Track cache copies' metadata
- Serialize conflicting requests

Challenges

1. Restricted expressive power

How to map coherence logic into switch pipelines ?



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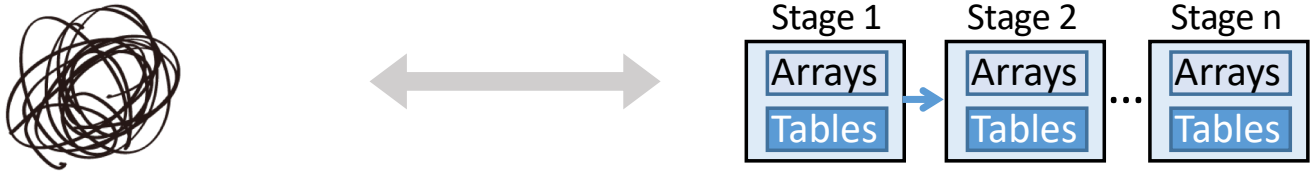

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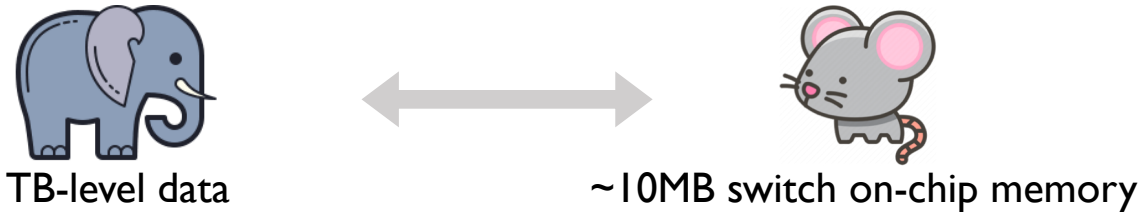
How to manage coherence of large amounts of data ?



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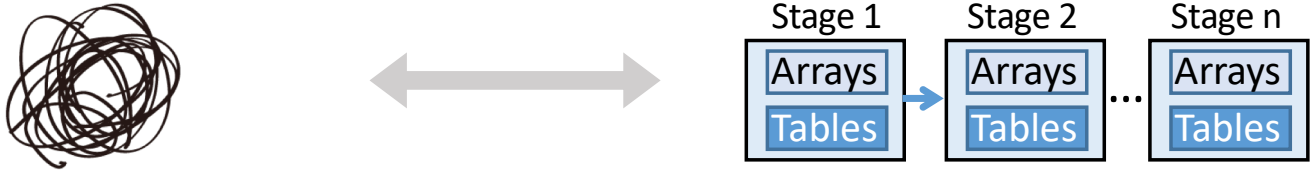

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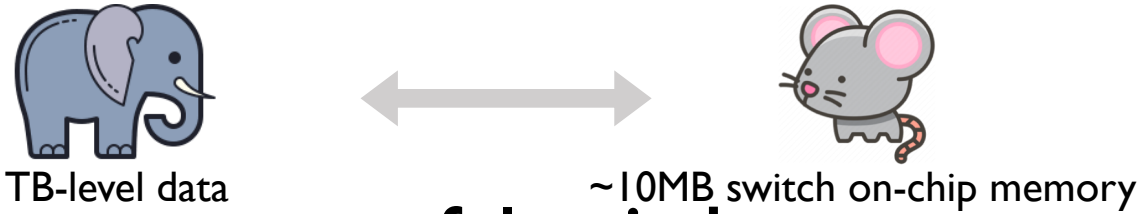
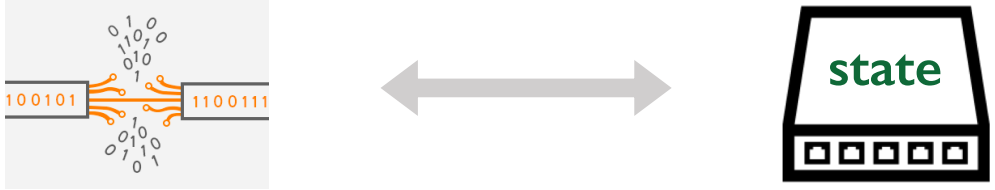


3. Packet loss upon stateful switch

How to enforce exactly-once semantics ?

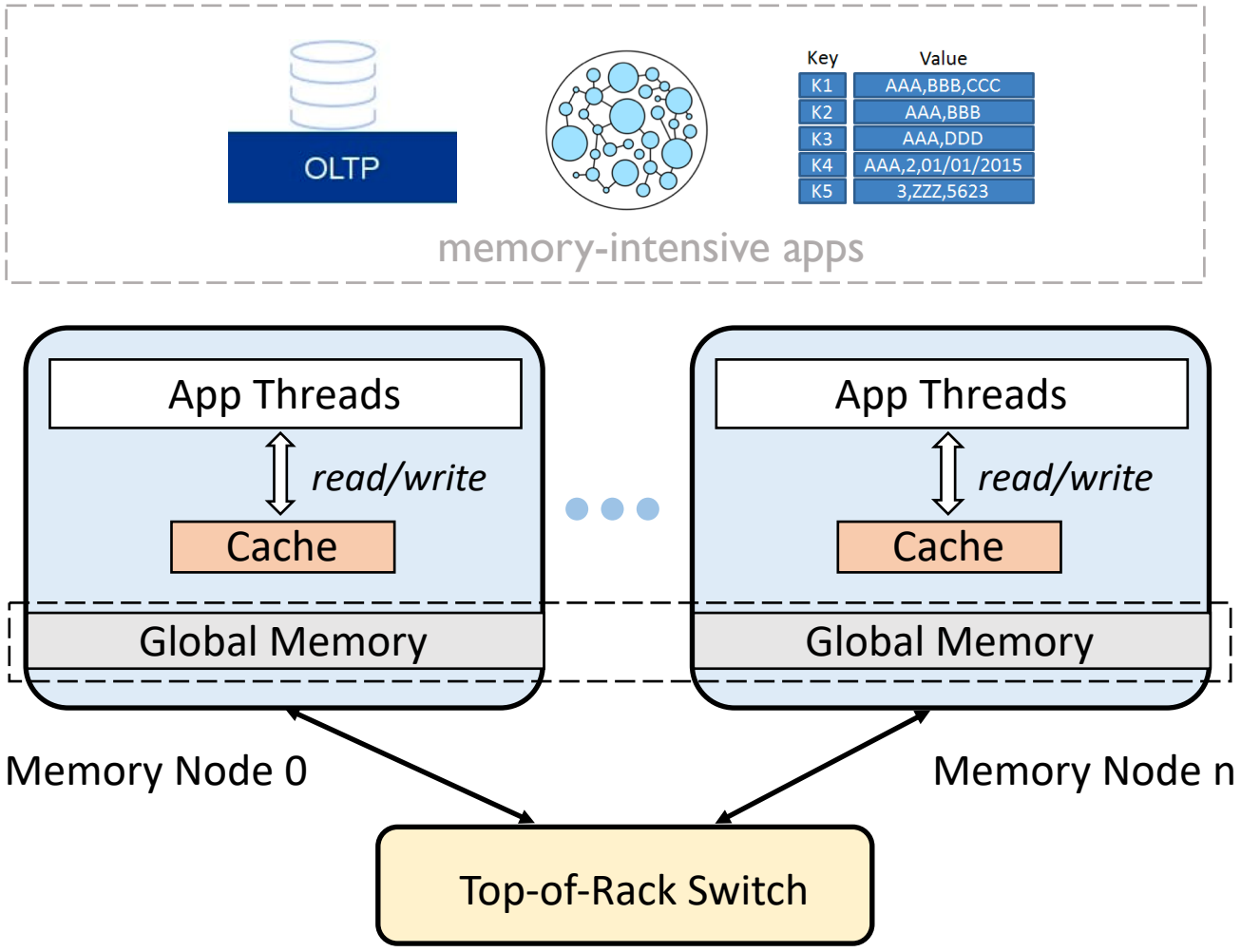


Outline

- Background & Motivation
- Concordia: a DSM with In-Network Coherence
- Results
- Summary & Conclusion

Concordia Architecture

A user-level rack-scale DSM



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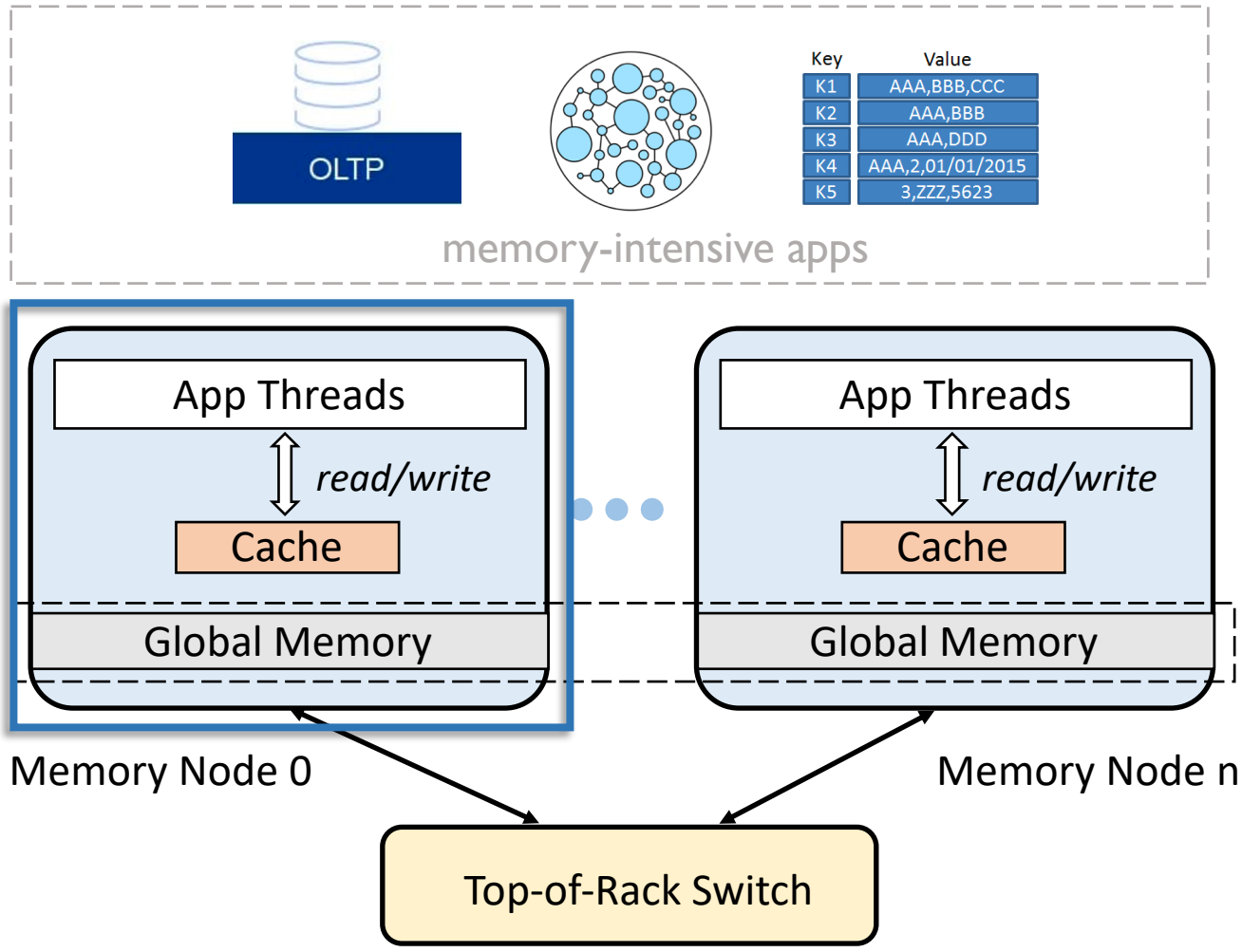

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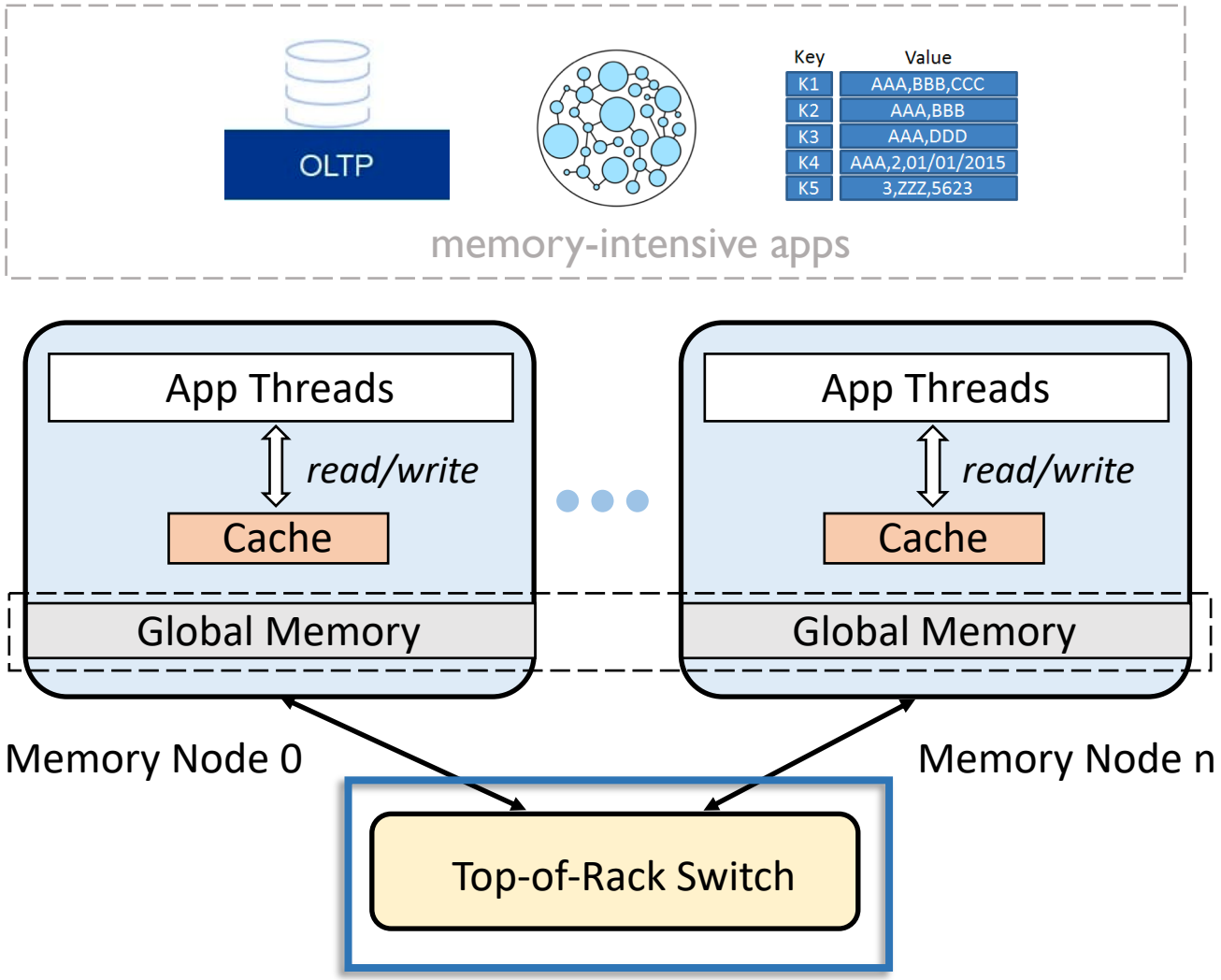
Top-of-rack switch

- Route normal packets
- Accelerate coherence



Concordia Architecture

Key Designs

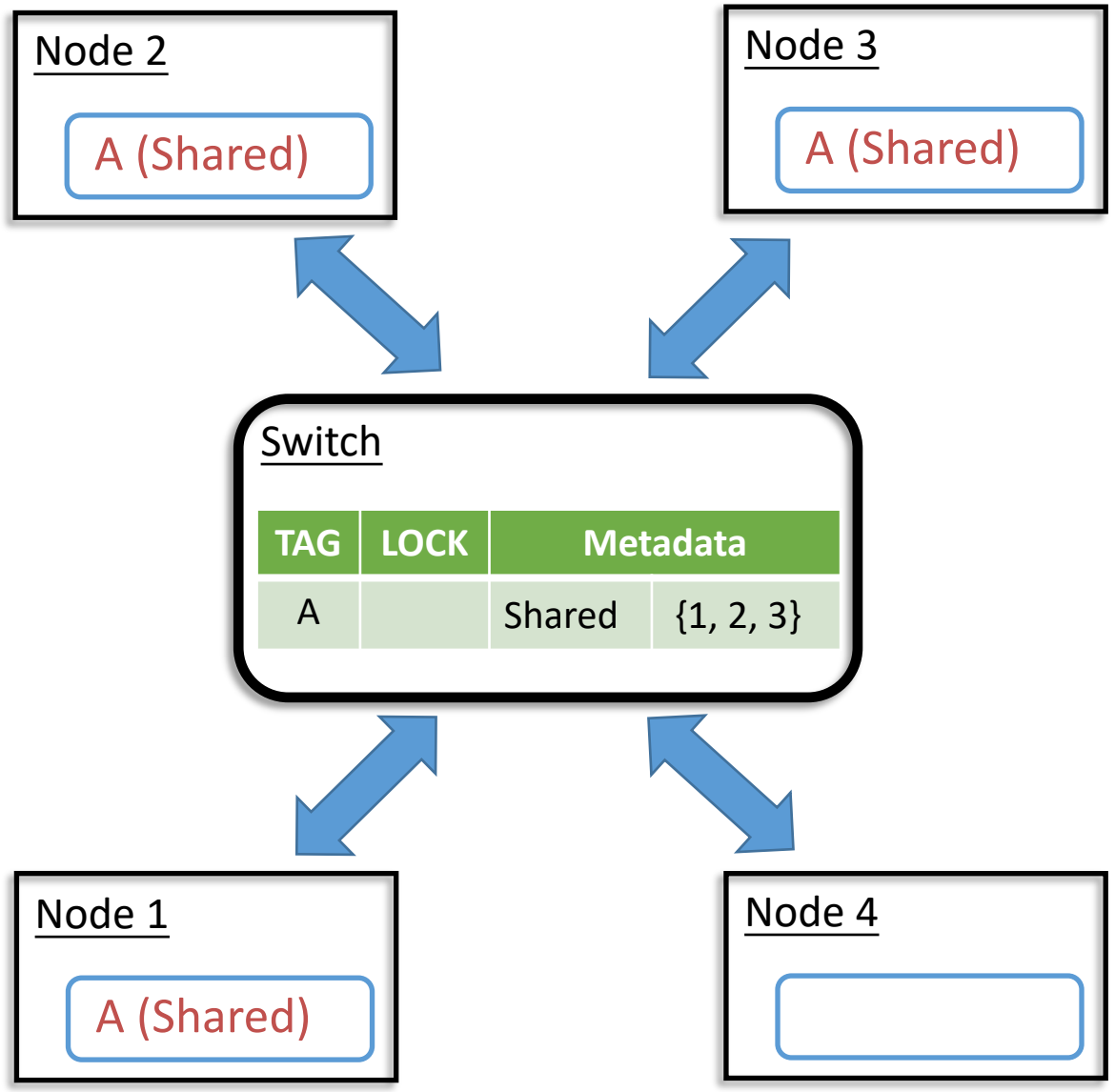
- 🌧️ Restricted expressive power
- ☀️ In-Network Coherence Protocol

- 🌧️ Limited switch memory
- ☀️ Ownership Migration

- 🌧️ Packet loss upon stateful switch
- ☀️ Idempotent Operations

In-Network Coherence Protocol

Write-invalidate protocol



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- Cache block metadata (status, sharers)
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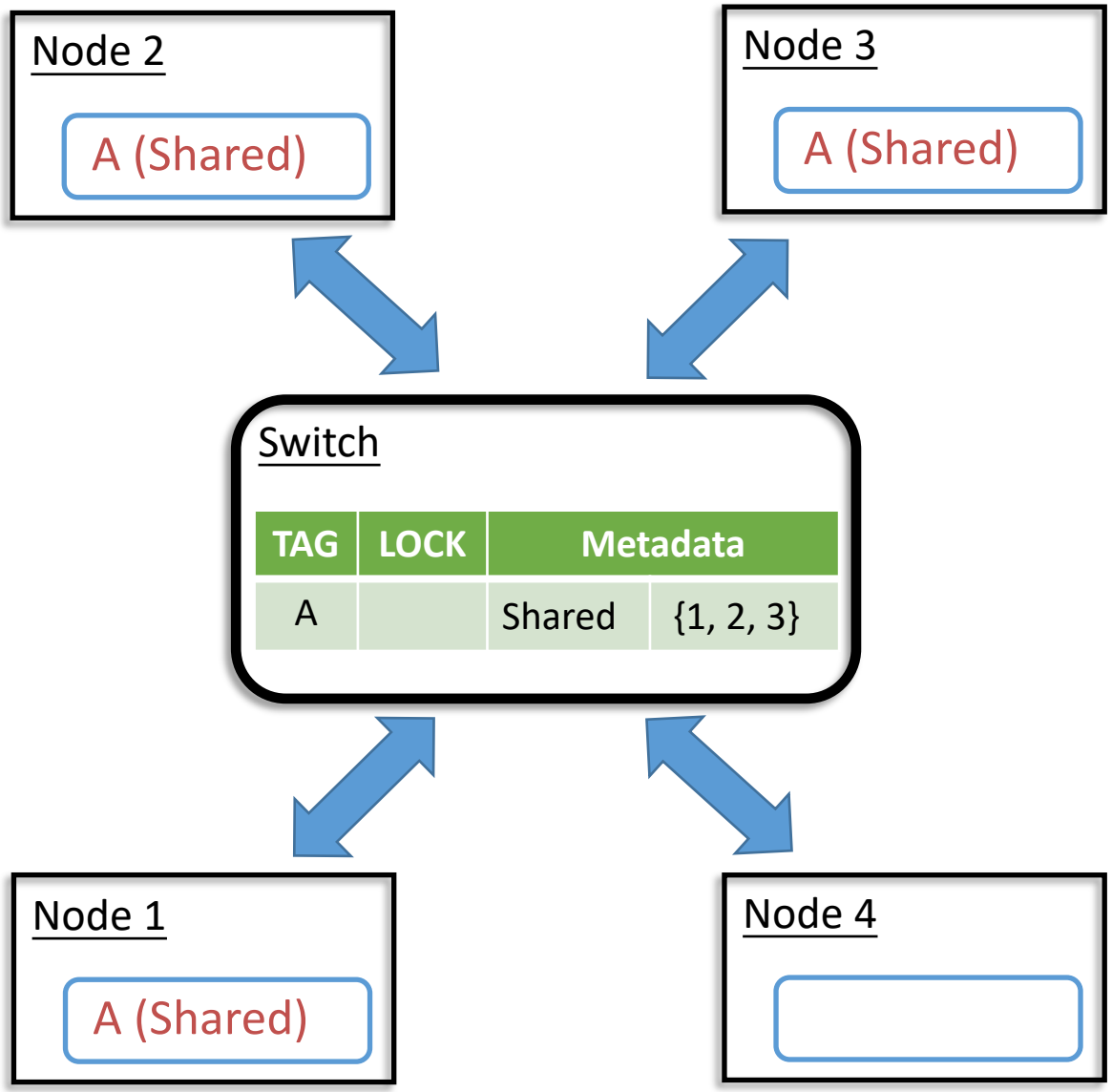

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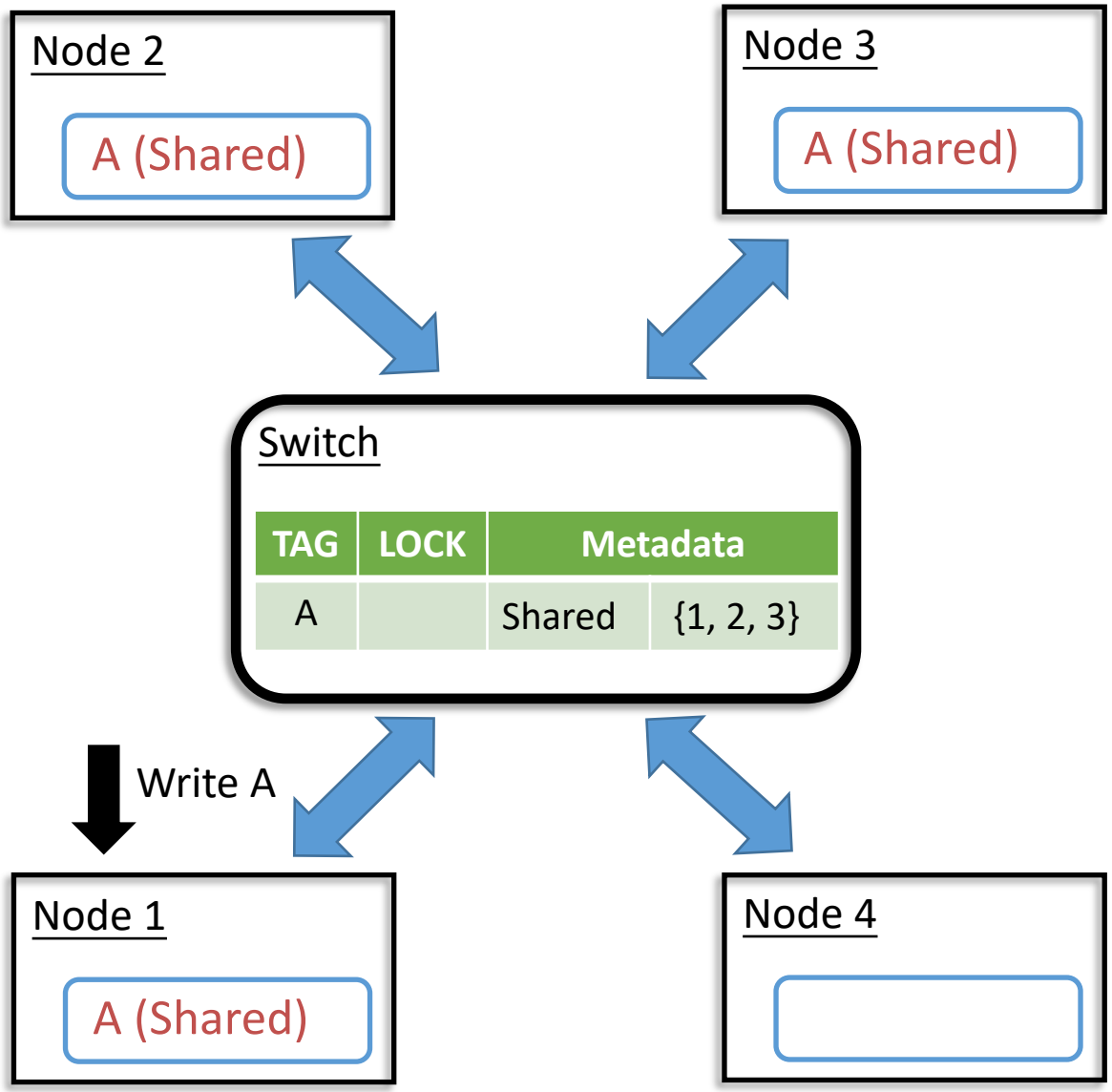

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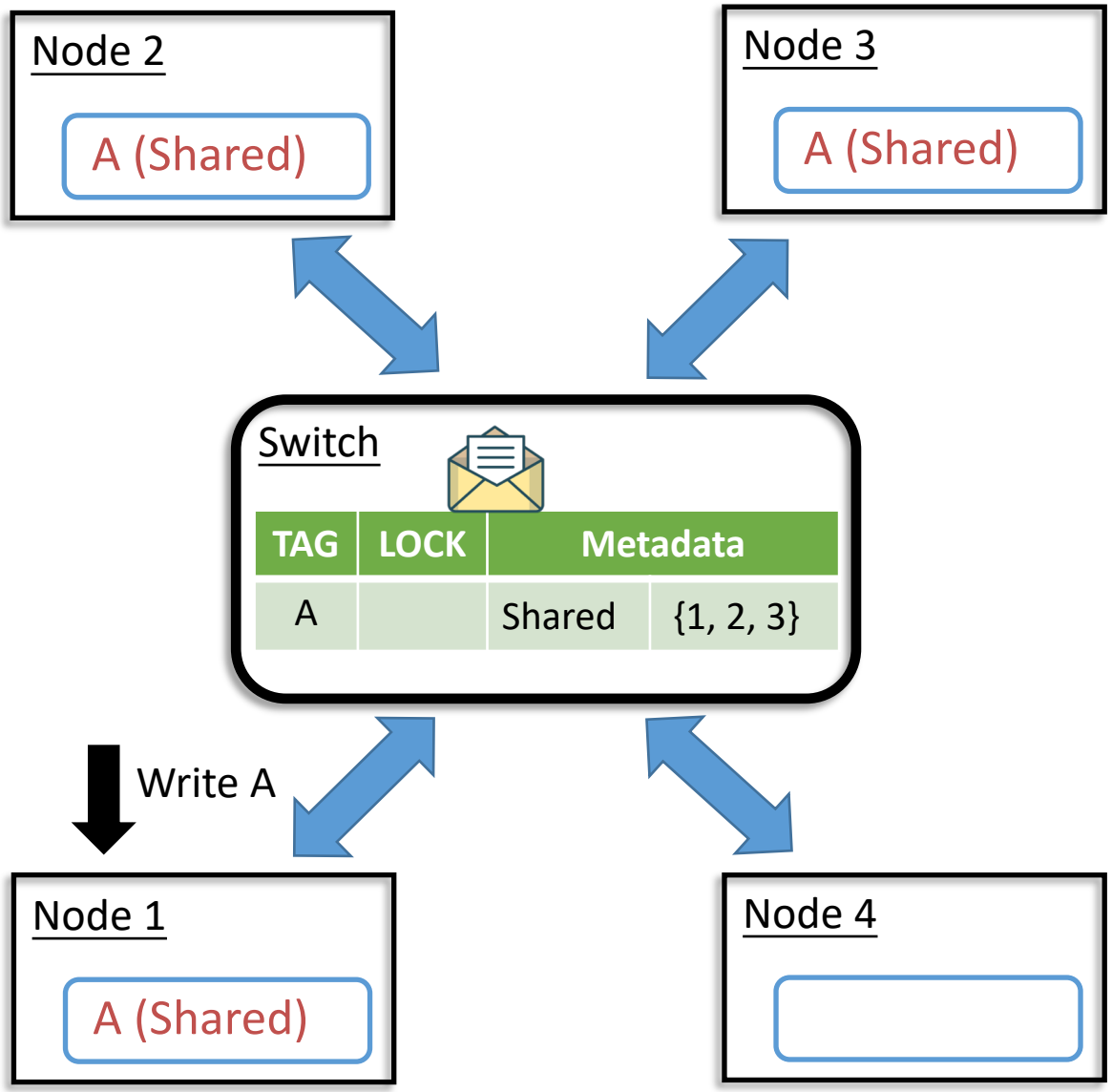

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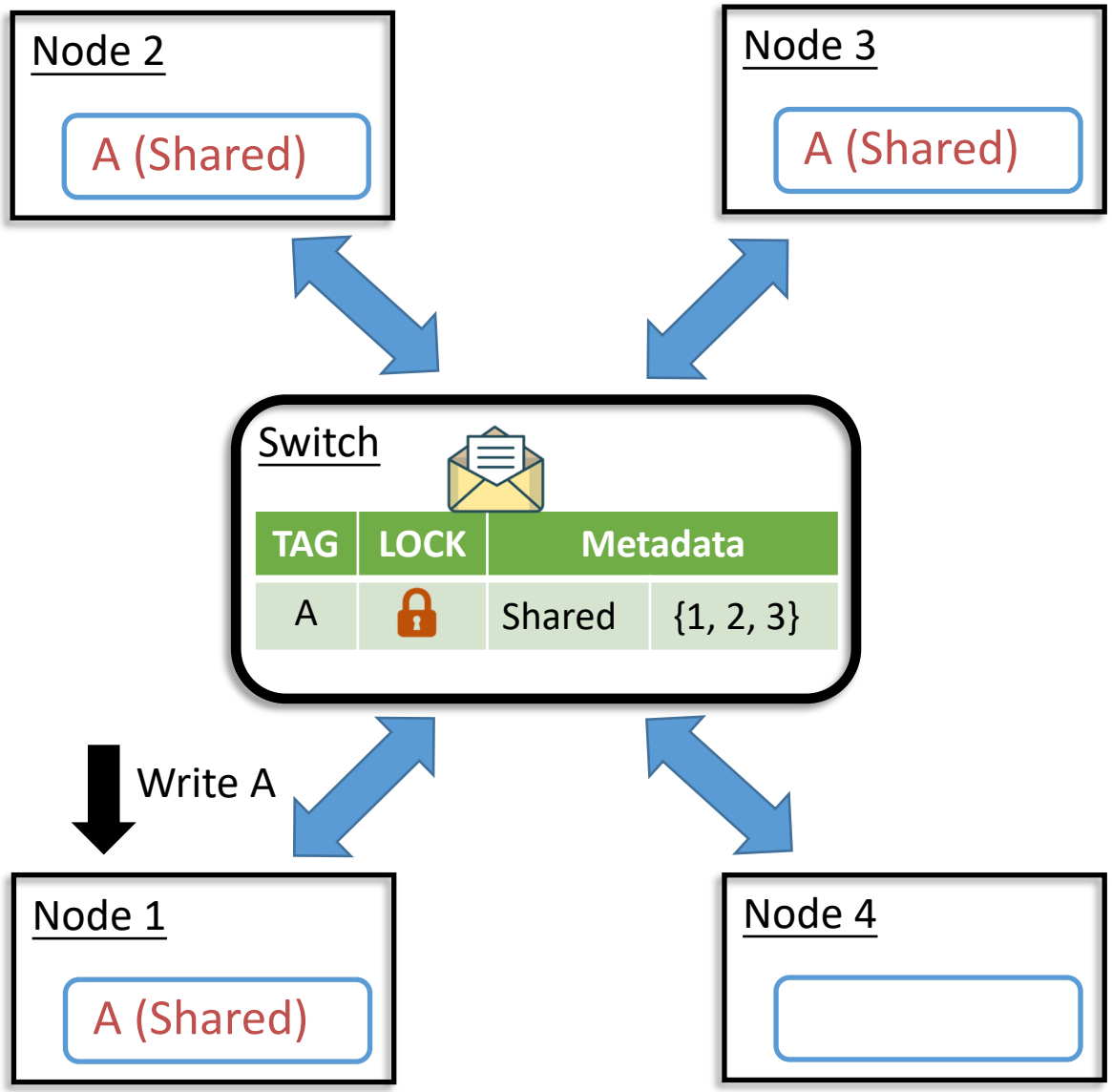

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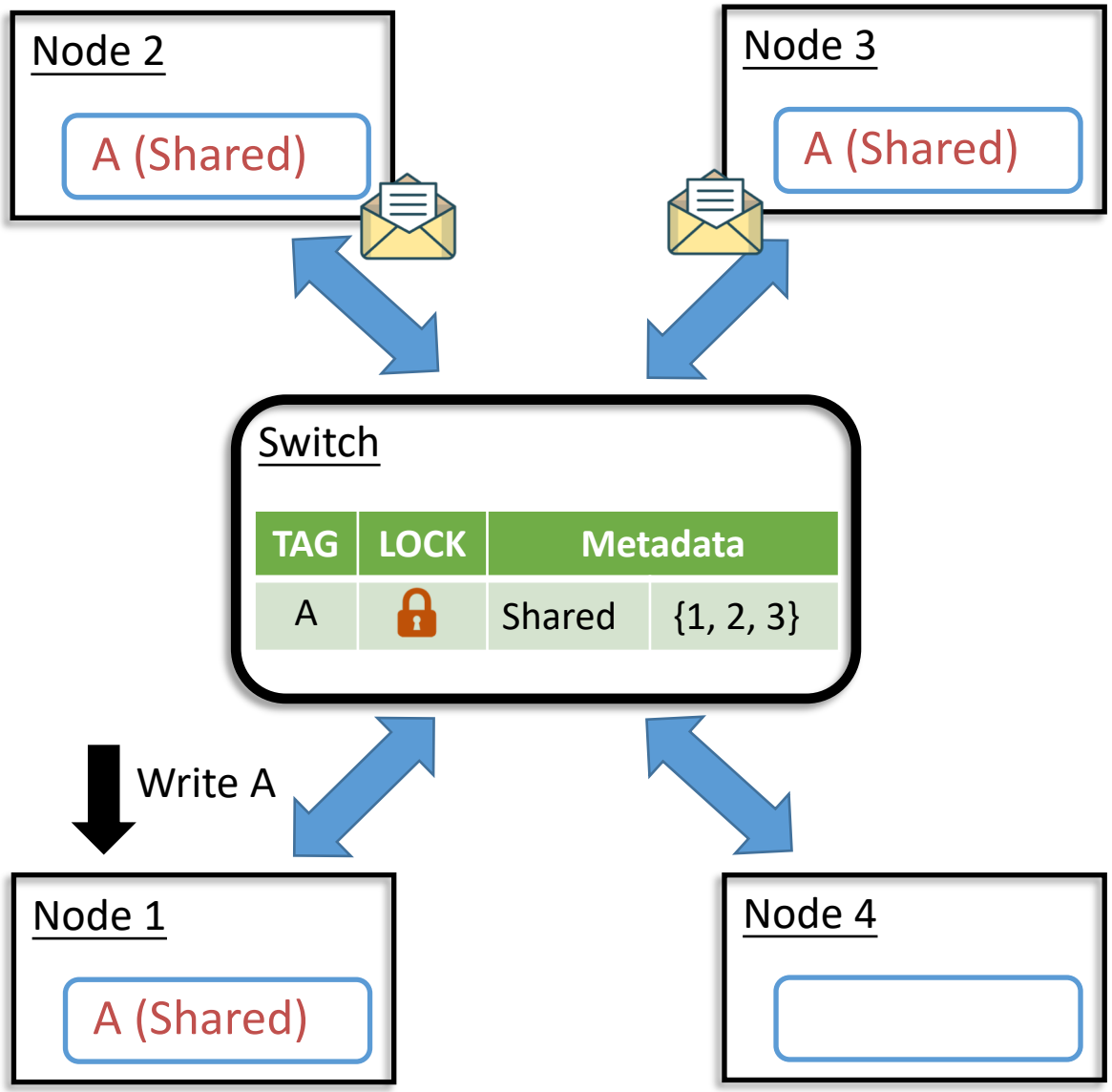

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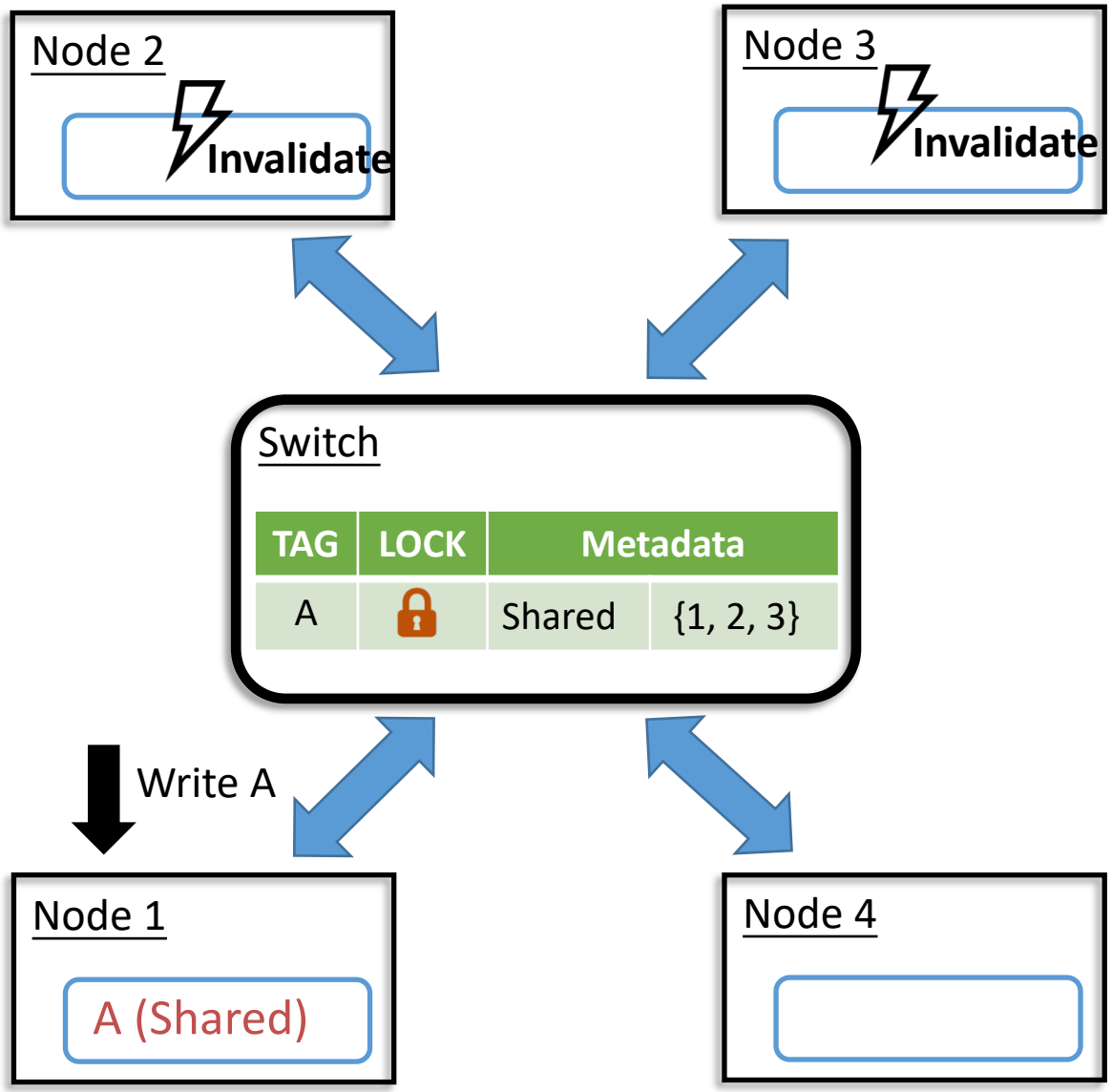

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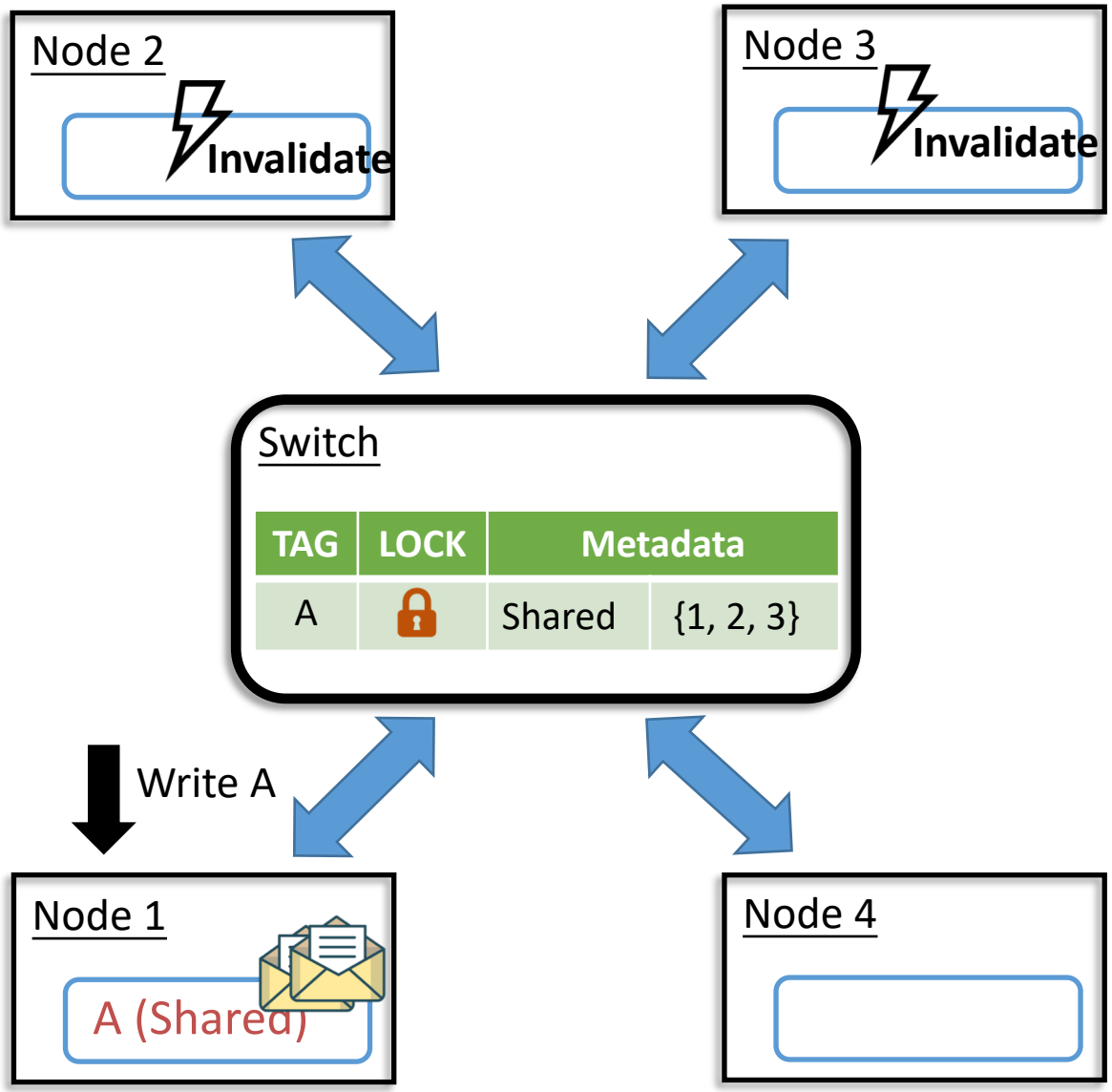

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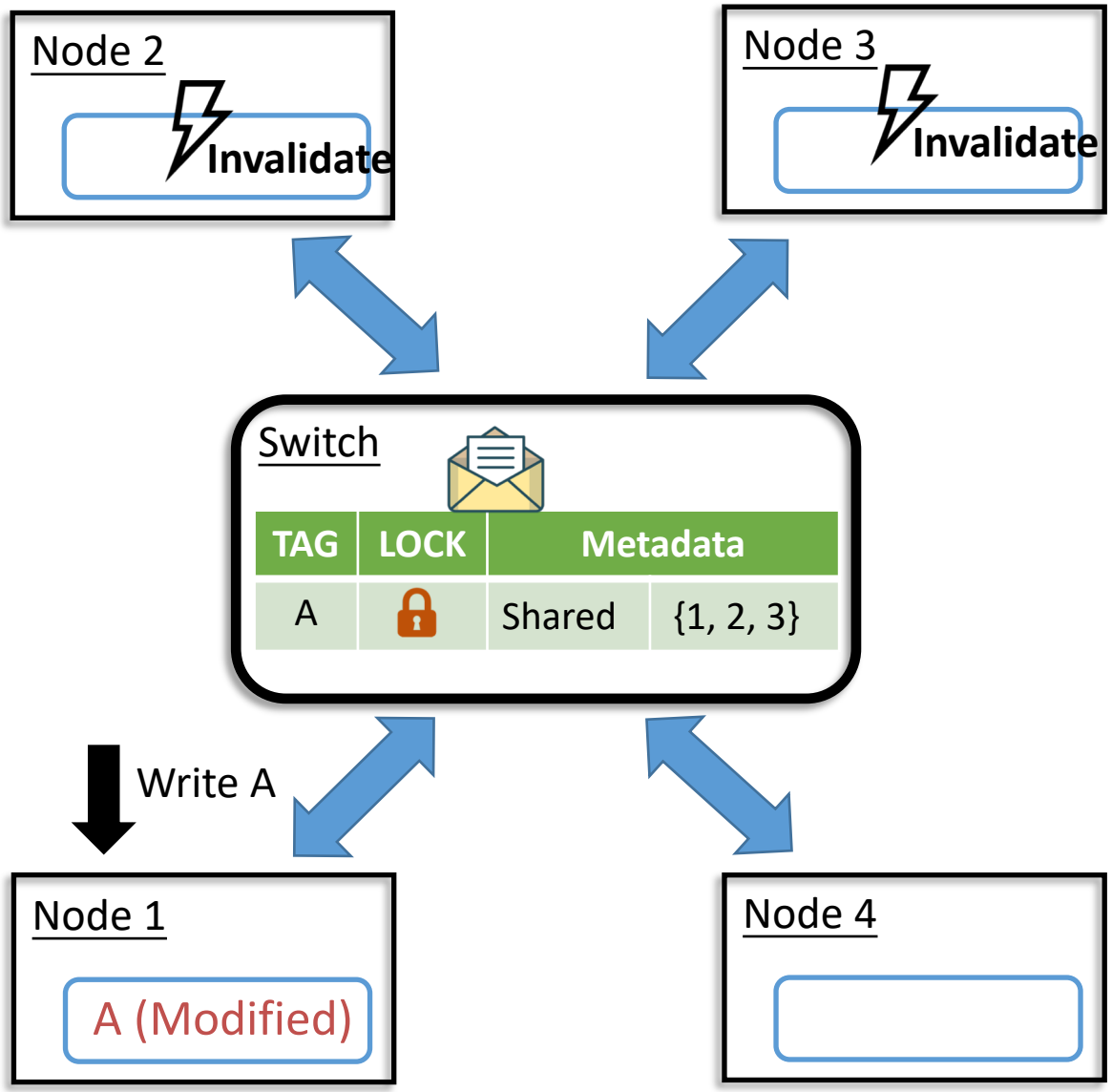

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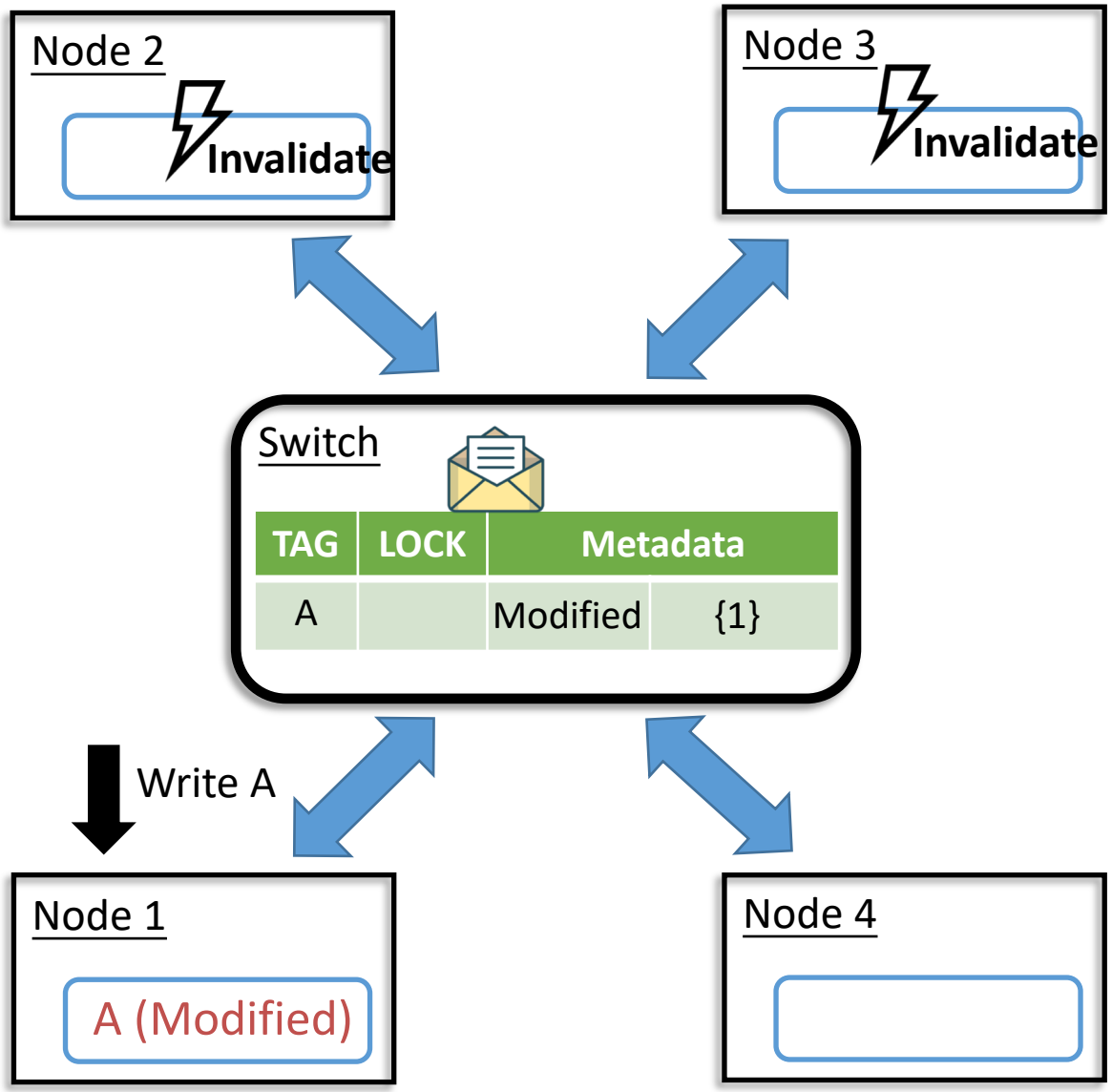

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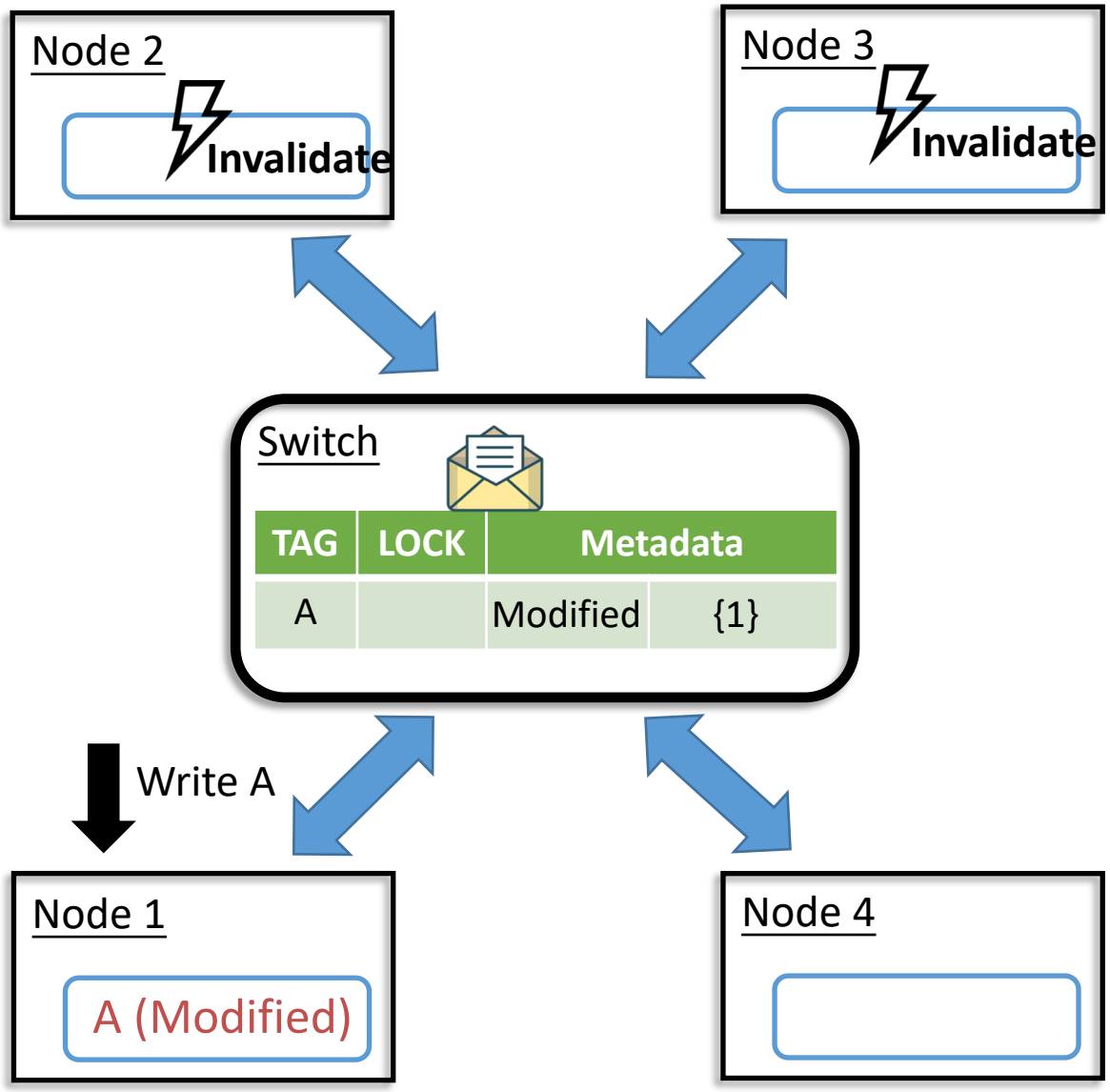
(1) 1 RTT (unlock is async)
(2) Minimized network traffic



Ownership Migration

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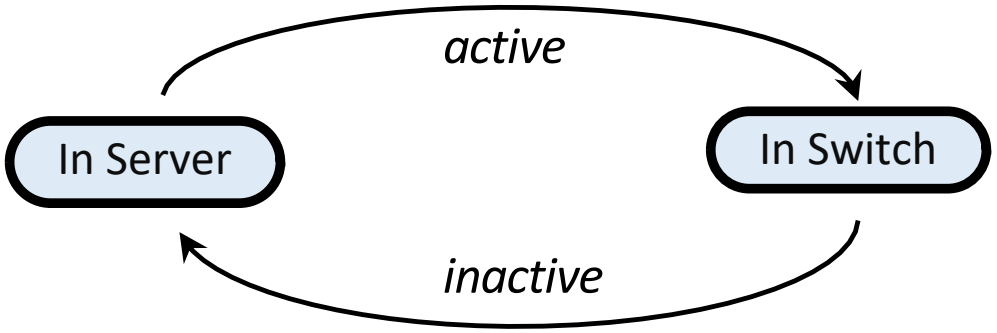

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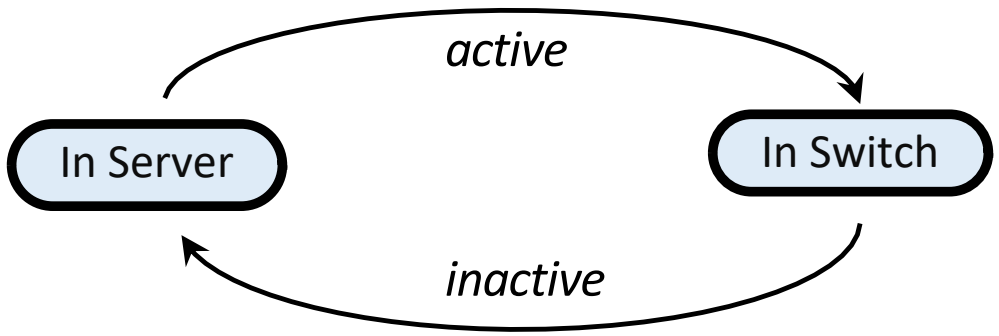
Ownership Migration

Limited switch memory cannot accommodate metadata of all cache blocks

The switch manages coherence of active cache blocks

Ownership Migration

- If a cache block triggers lots of invalidations, migrate its ownership: Servers → Switch
- If a cache block is inactive, migrate its ownership: Switch → Servers



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- Servers record SNs of executed requests,
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Switch Idempotence

- For each app thread, the switch records whether it holds lock, to avoid deadlock and repeated unlock

More details: checkout our paper

- Design details
  - Switch data plane design
  - Cases of different requests (e.g., cache eviction)
  - Handling failures of different components
  - Correctness proof
  - Corner cases of ownership migration
- Implementation details
  - Network stack (RDMA)
  - Cache organization (set-associative)
  - Global memory allocation (two-level allocation)
  - Synchronization primitive (rwlock)

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Experimental Setup

Hardware Platform

Server * 8

CPU	2 Intel Xeon E5-2650 CPUs
NIC	100Gbps Mellanox ConnectX-5
OS	CentOS 7.4 , Linux kernel 3.10.0

Programmable Switch * 1

Type	Barefoot Tofino switch
Port	32 * 100Gbps
SW	bf-sde-8.2.0

Experimental Setup

Hardware Platform

Server * 8

CPU	2 Intel Xeon E5-2650 CPUs
NIC	100Gbps Mellanox ConnectX-5
OS	CentOS 7.4 , Linux kernel 3.10.0

Programmable Switch * 1

Type	Barefoot Tofino switch
Port	32 * 100Gbps
SW	bf-sde-8.2.0

Compared DSMs

Grappa [ATC'15]	No caching, ship computation, RDMA-based
GAM [VLDB'18]	Caching, directory-based coherence, RDMA-based
Concordia-base	Servers manage coherence of all cache blocks

Experimental Setup

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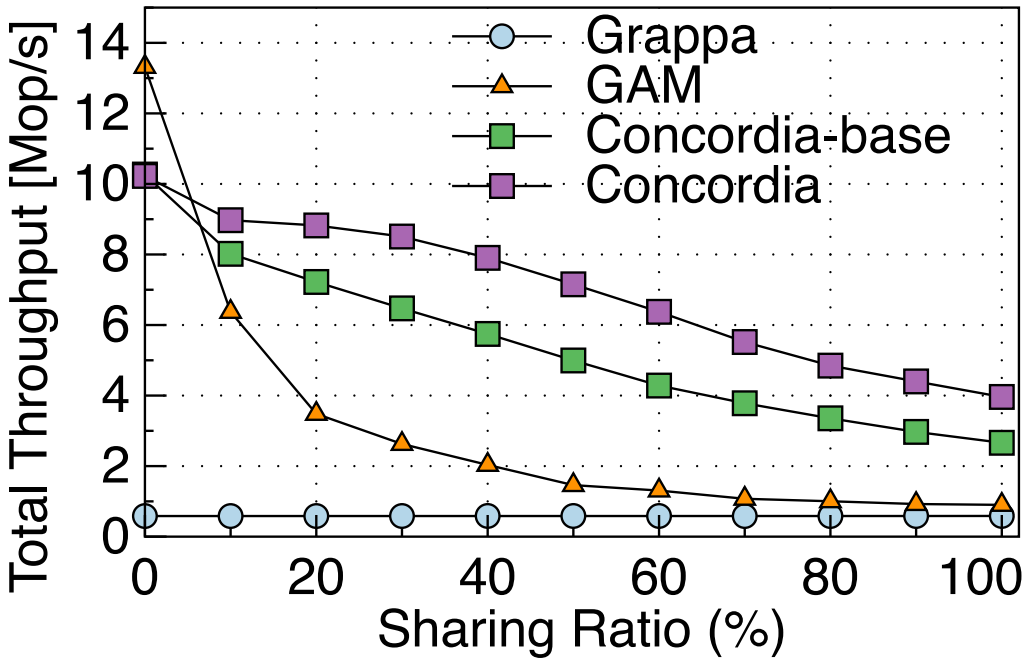
Benchmark

- Micro benchmarks (sharing ratio, locality ratio, reading ratio…)
- Applications (key-value store, transaction, graph computation)

Micro Benchmarks



(A) Throughput

4 app threads per node,

8-bytes writes/reads (1:1), No locality

8GB working set, 1GB cache, 250MB shared areas

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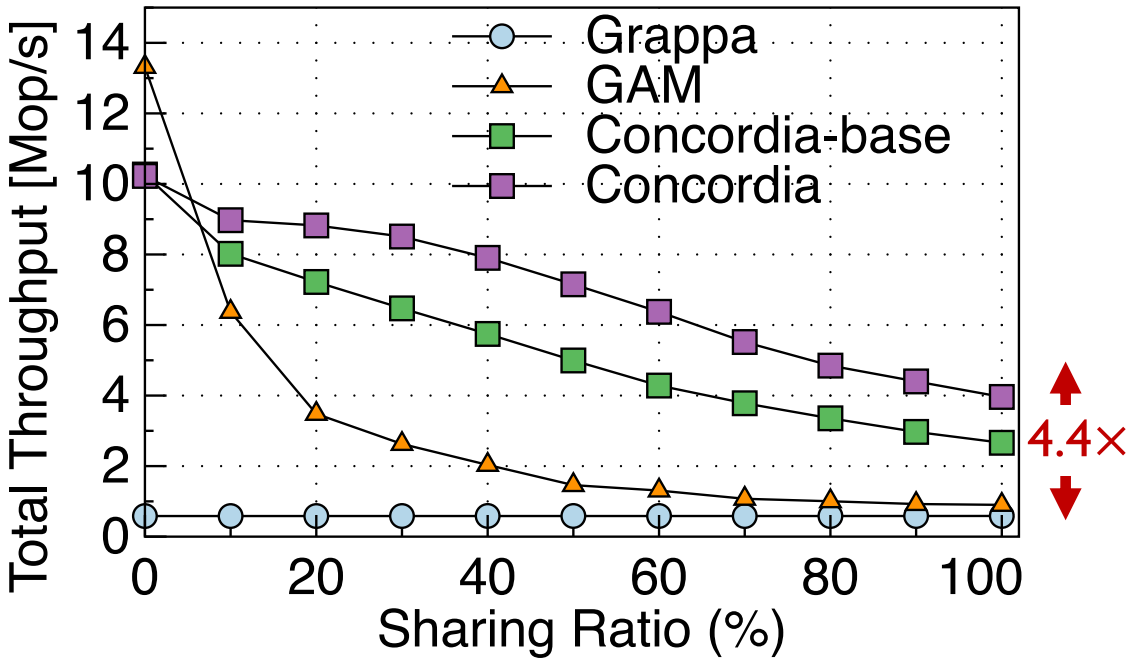

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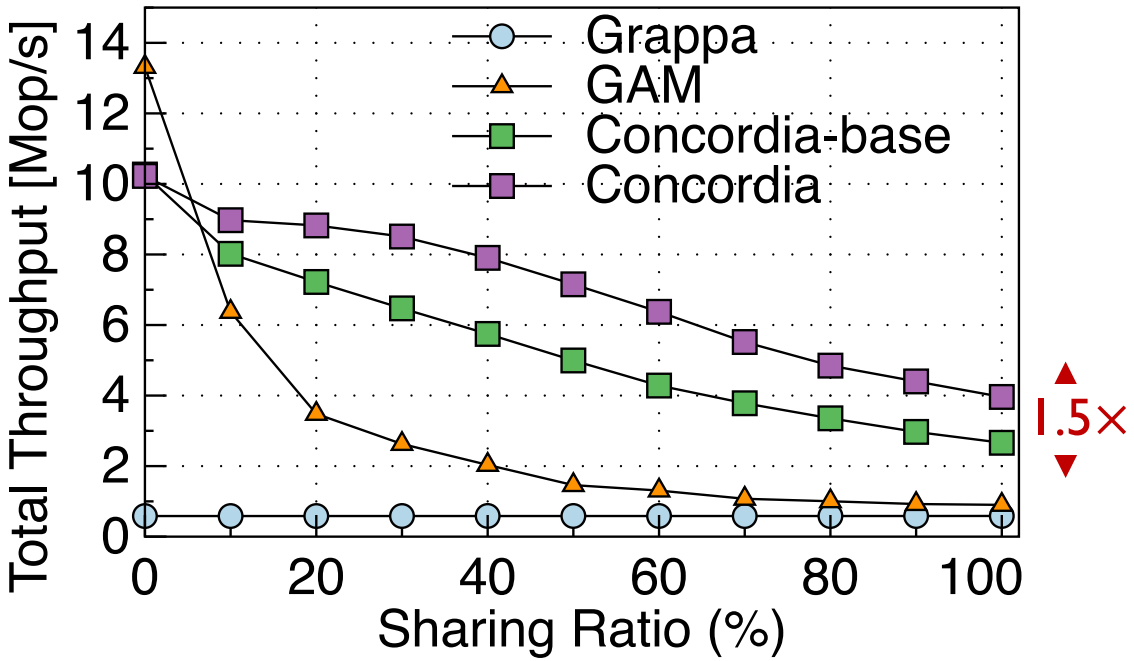

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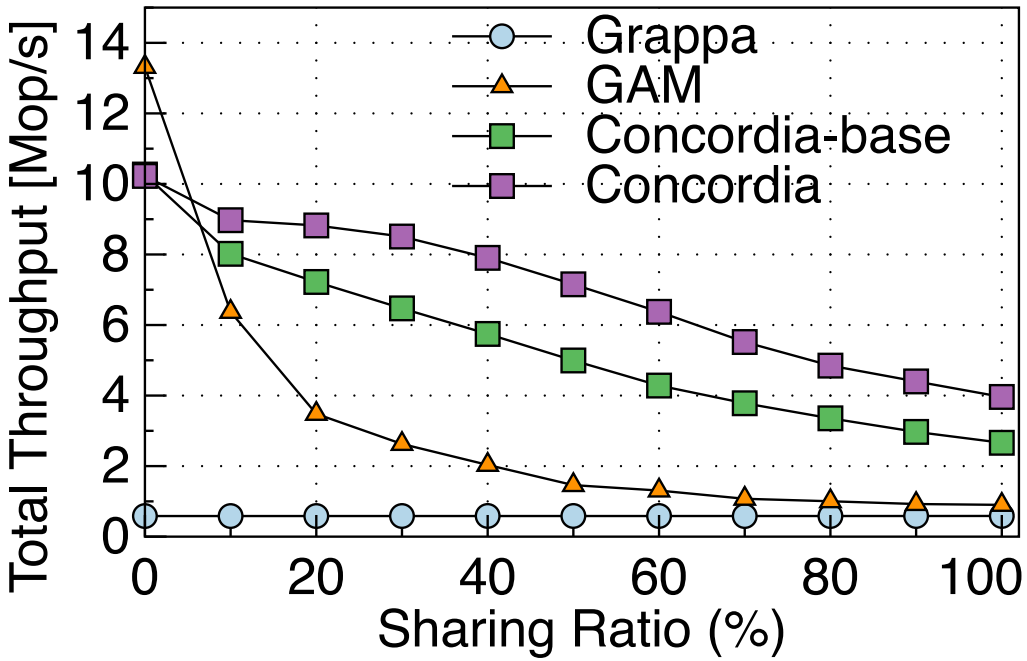

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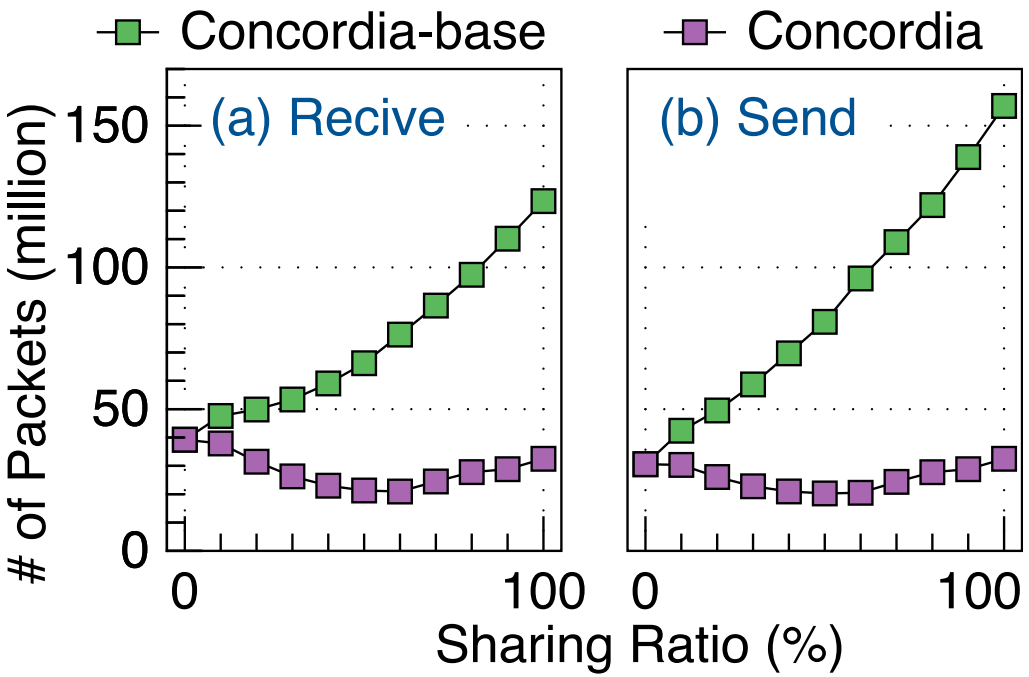

(B) Packets received/sent by servers

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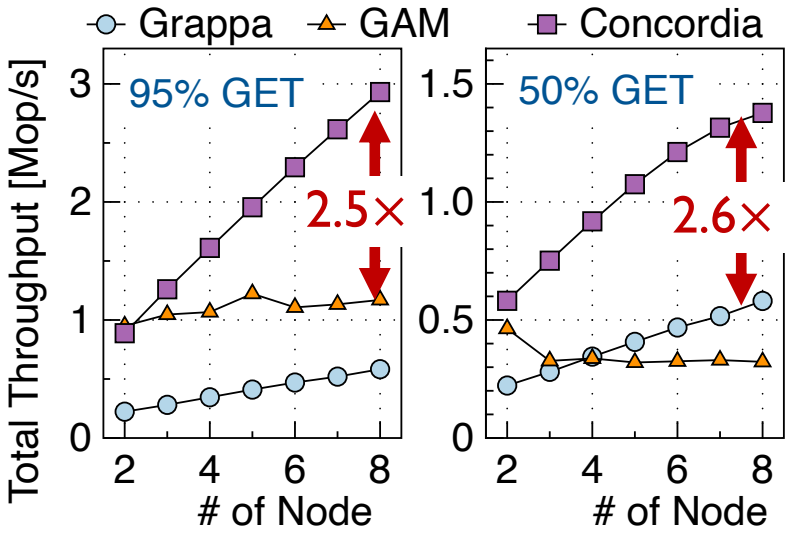
Concordia effectively reduces network traffic

Applications

- Zipfan 0.99
- 8-byte key, 128-byte value
- Hash table index



(A) Key-value Store (YCSB-like)

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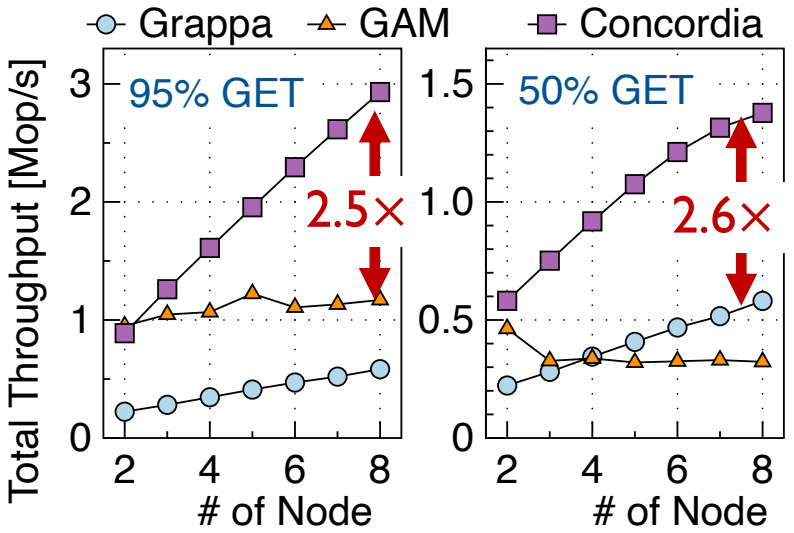
- Ported from GAM
- Share everything
- 32 warehouses



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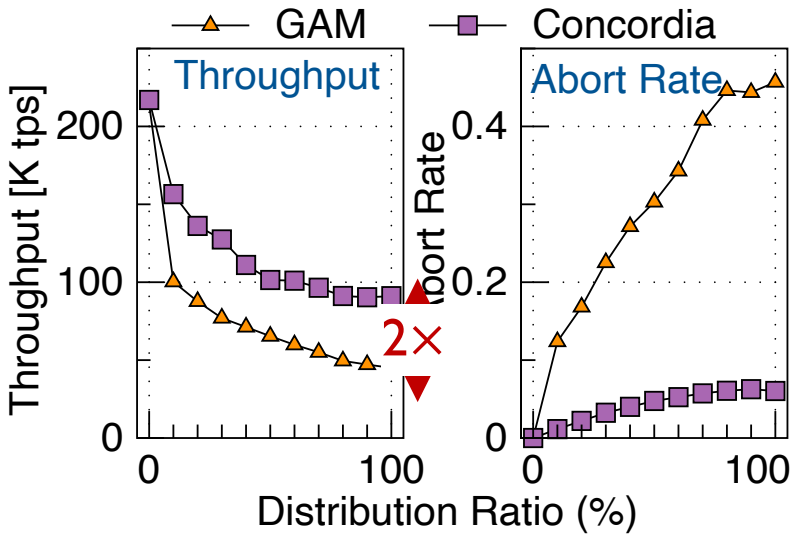

(B) Transaction (TPCC)

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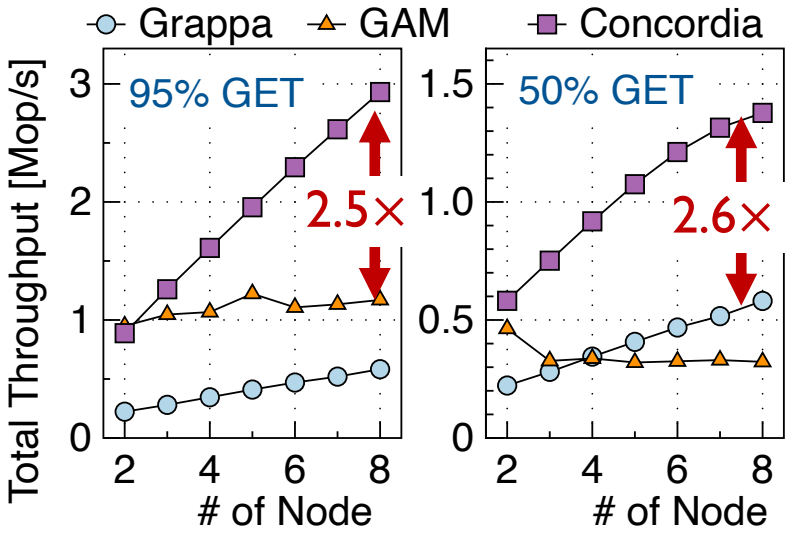

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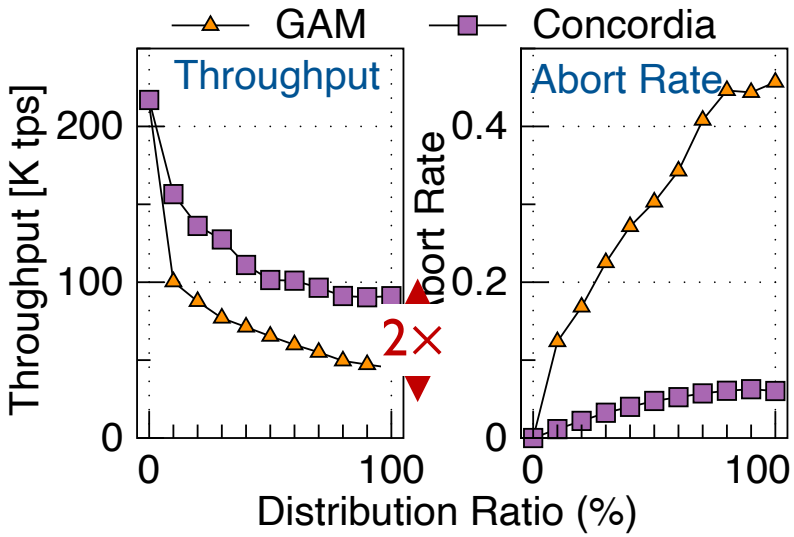
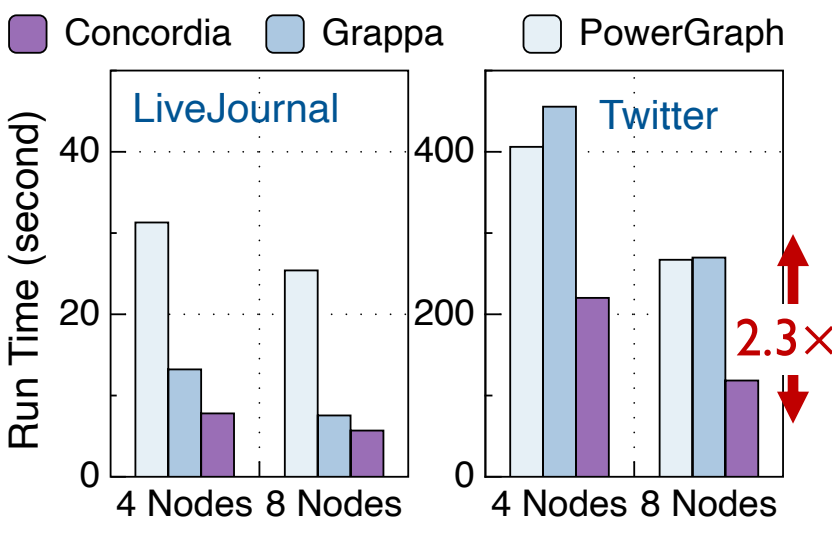


(B) Transaction (TPCC)

- Vertex-centric
- Gather, apply and scatter
- Two dataset



(C) Graph Comp (PageRank)

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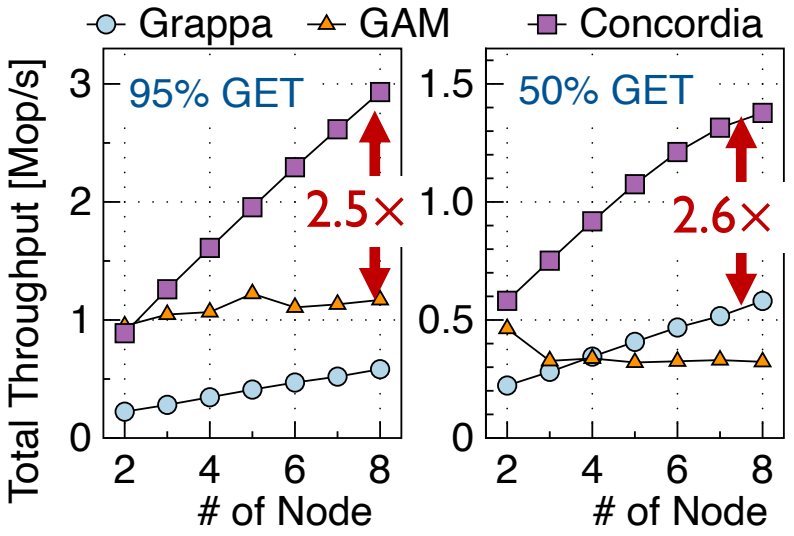

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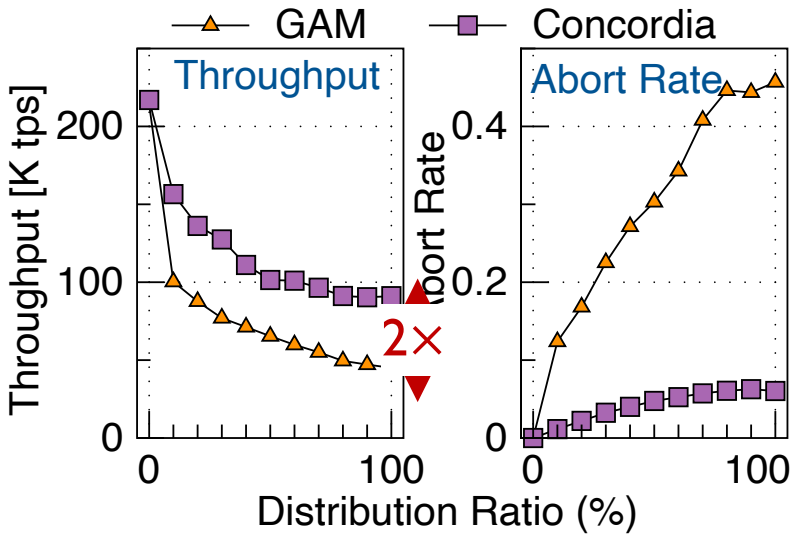

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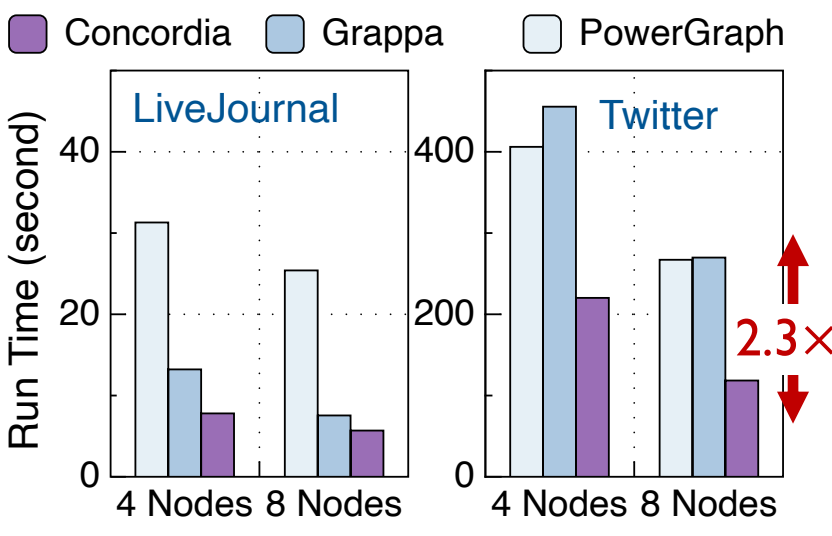

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Concordia supports various applications, and boosts their performance

Outline

- Background & Motivation
- Concordia: a DSM with In-Network Coherence
- Results
- Summary & Conclusion

Summary & Conclusion

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  - Ownership migration
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  - Idempotent operations
- Results
  - Concordia outperforms state-of-the-arts
  - Concordia underpins various applications

Thanks & QA

Concordia: Distributed Shared Memory with In-Network Cache Coherence

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