

Varys

Protecting SGX Enclaves From Practical Side-Channel Attacks

Oleksii Oleksenko, Bohdan Trach

Robert Krahn, Andre Martin, Christof Fetzer

Mark Silberstein



Key issue of the cloud:

We cannot trust it

We cannot trust the cloud

- Thousands of employees
- Legal obligations
- Infrastructure vulnerabilities

GERALD SAUER OPINION 02.28.17 10:00 AM

A MURDER CASE TESTS ALEXA'S DEVOTION TO YOUR PRIVACY

Patch alert! Easy-to-exploit flaw in Linux kernel rated 'high risk'

Urgent security triage needed

Cloud Data Leak Exposes Information on 123 Million Americans

By: Sean Michael Kerner | December 20, 2017

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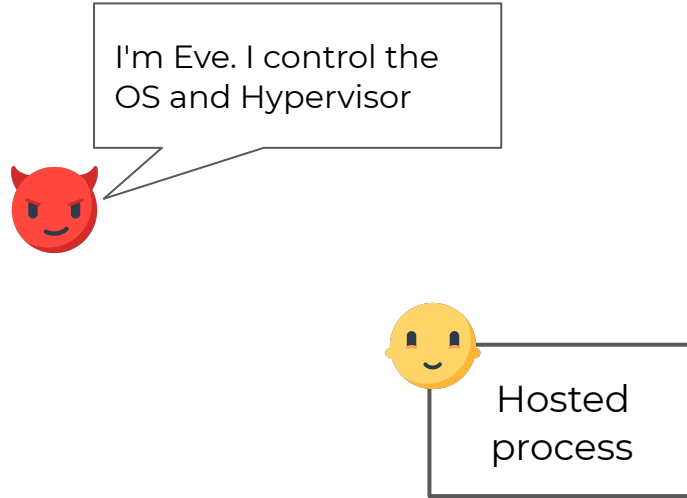
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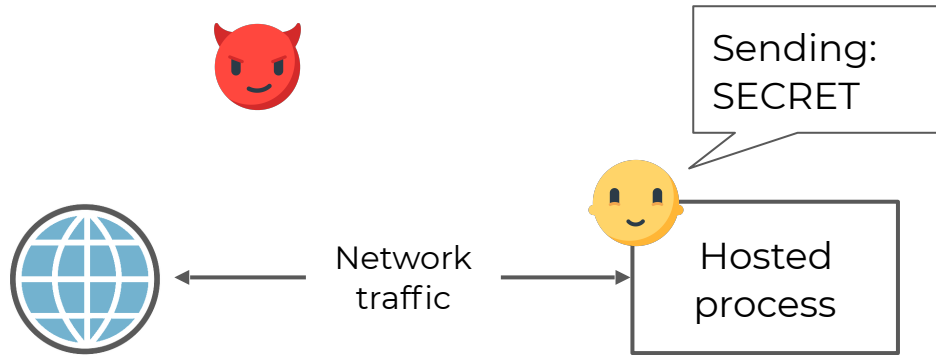
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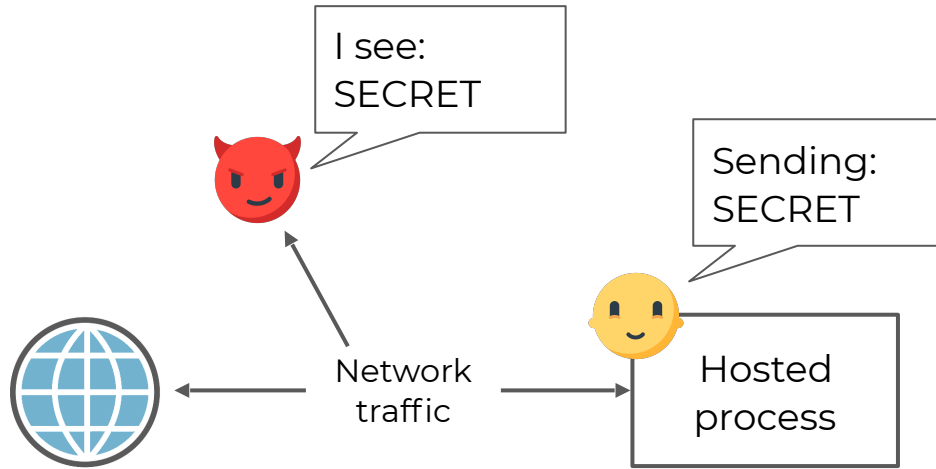
Privileged attack vectors



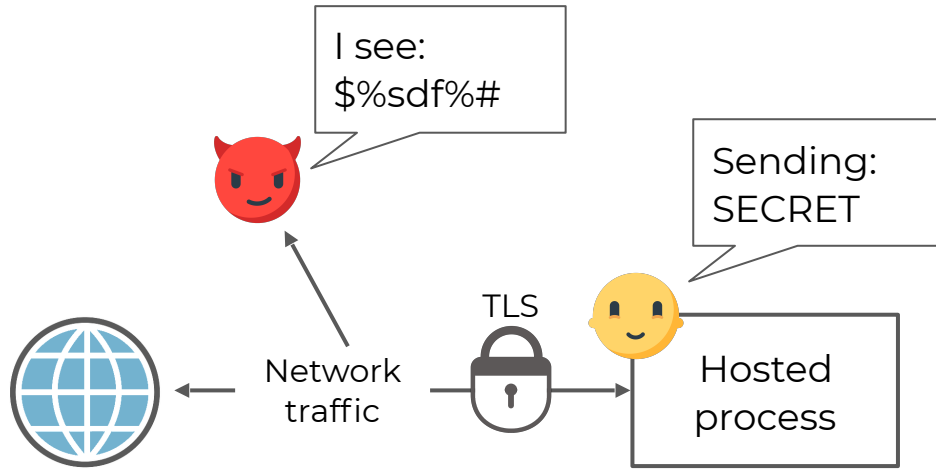
Privileged attack vectors: Network



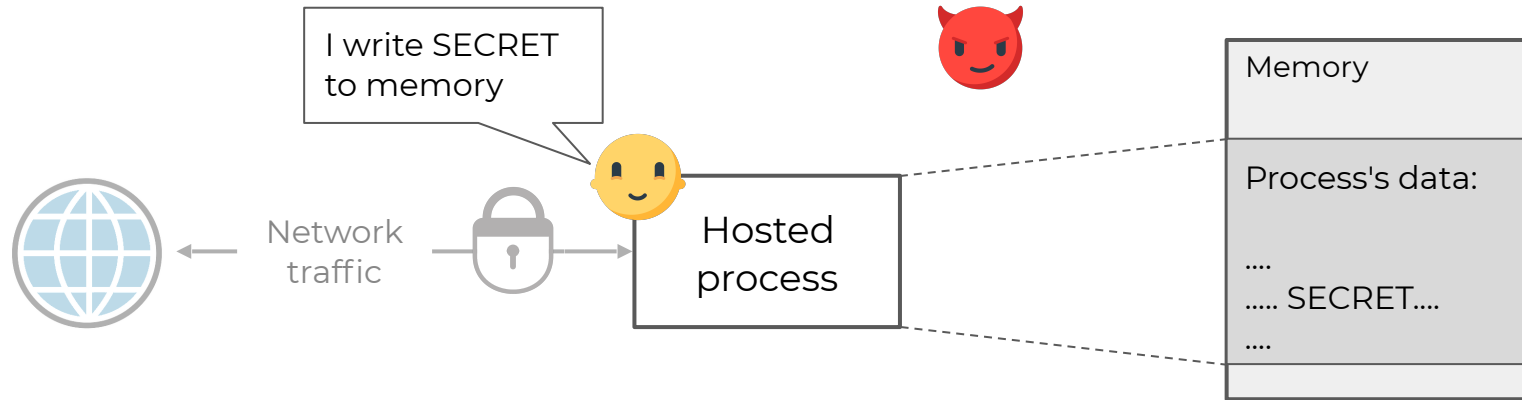
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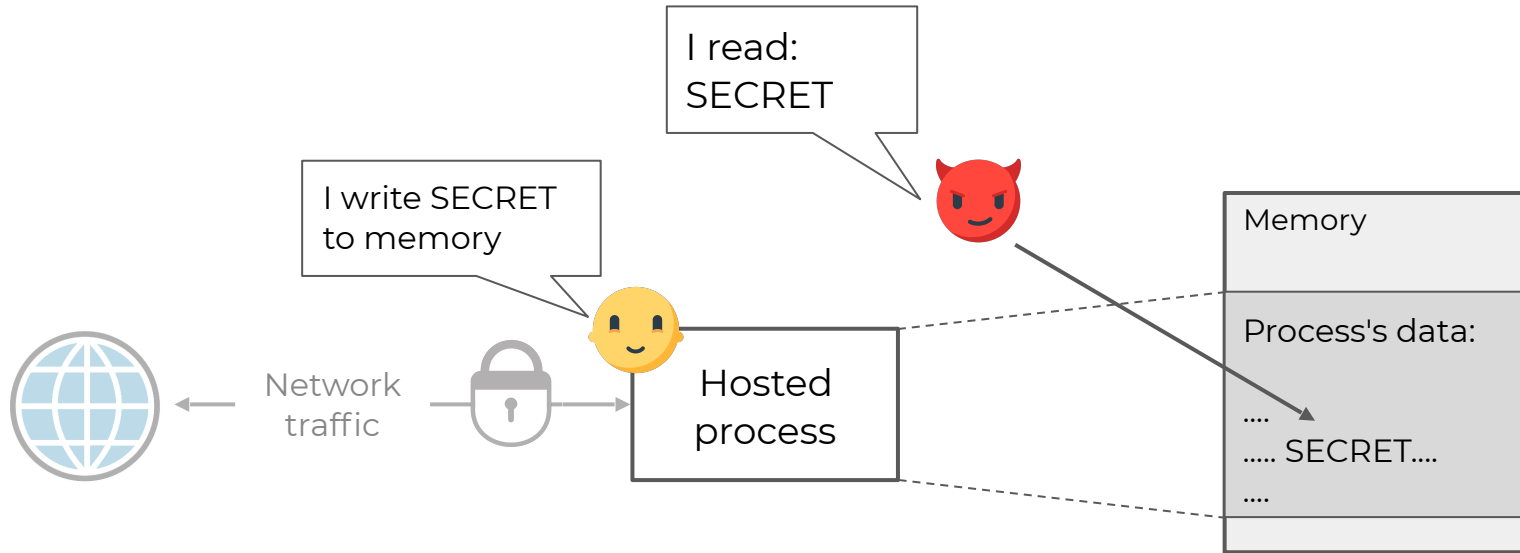
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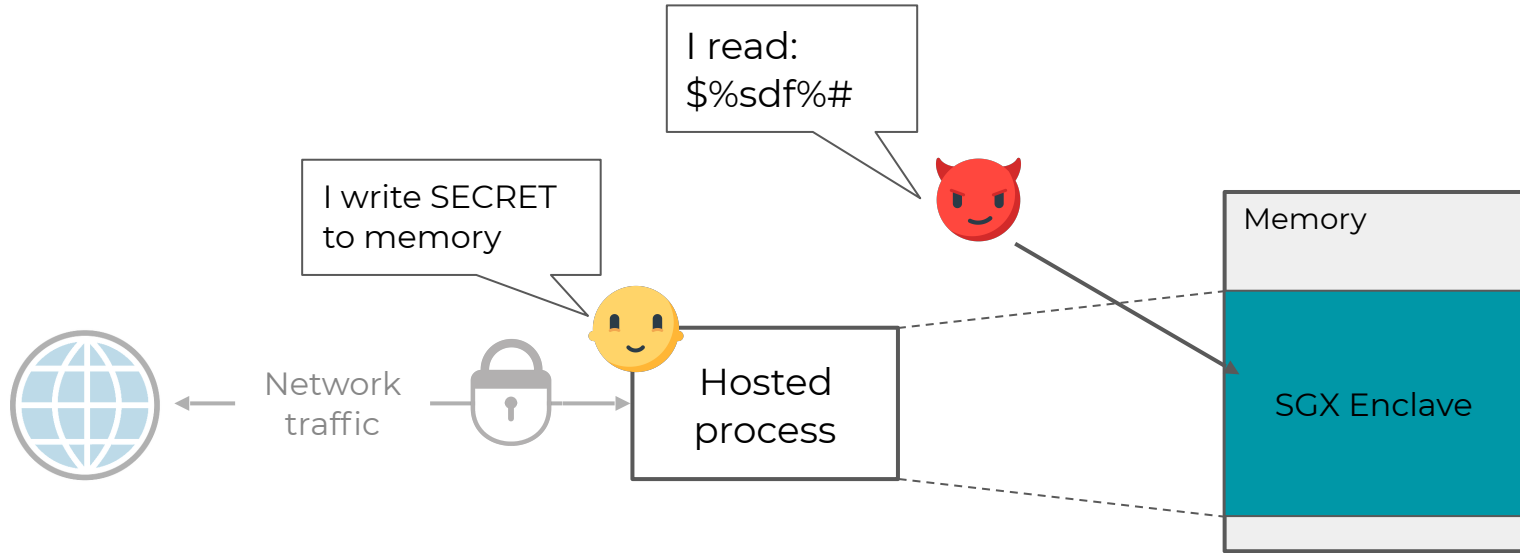
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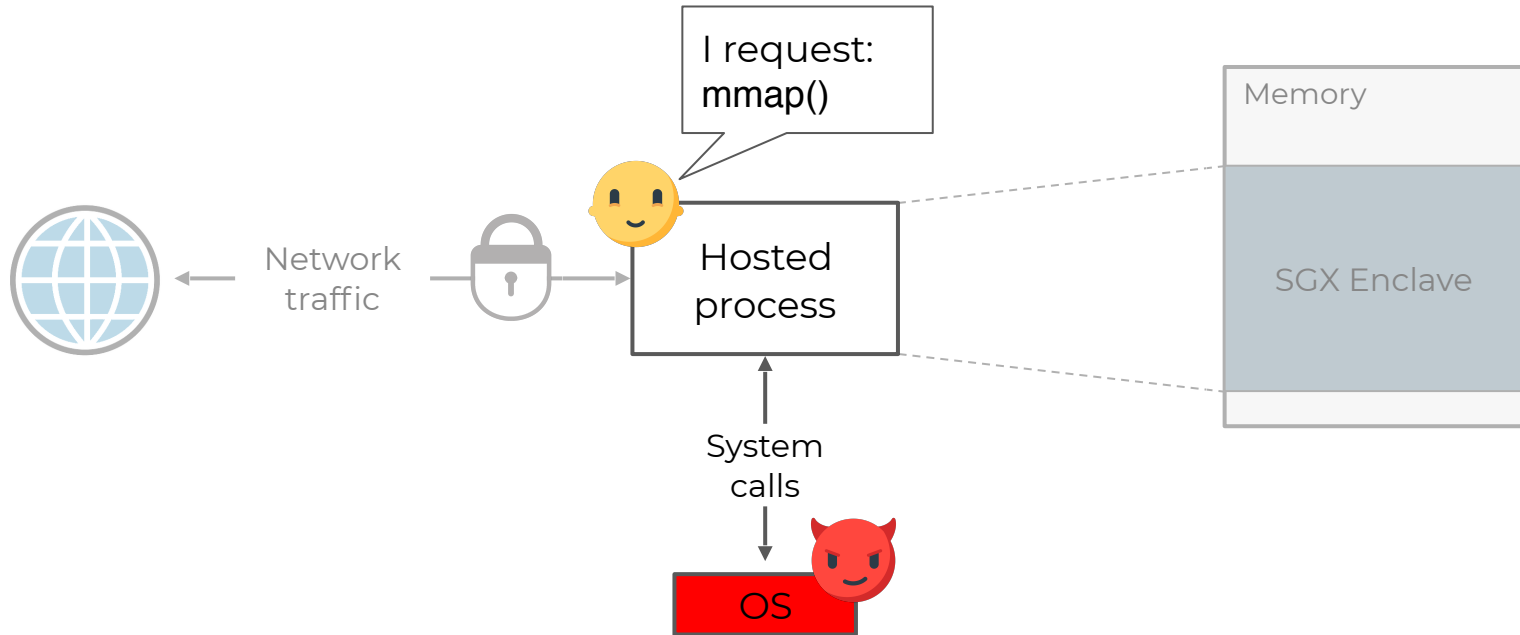
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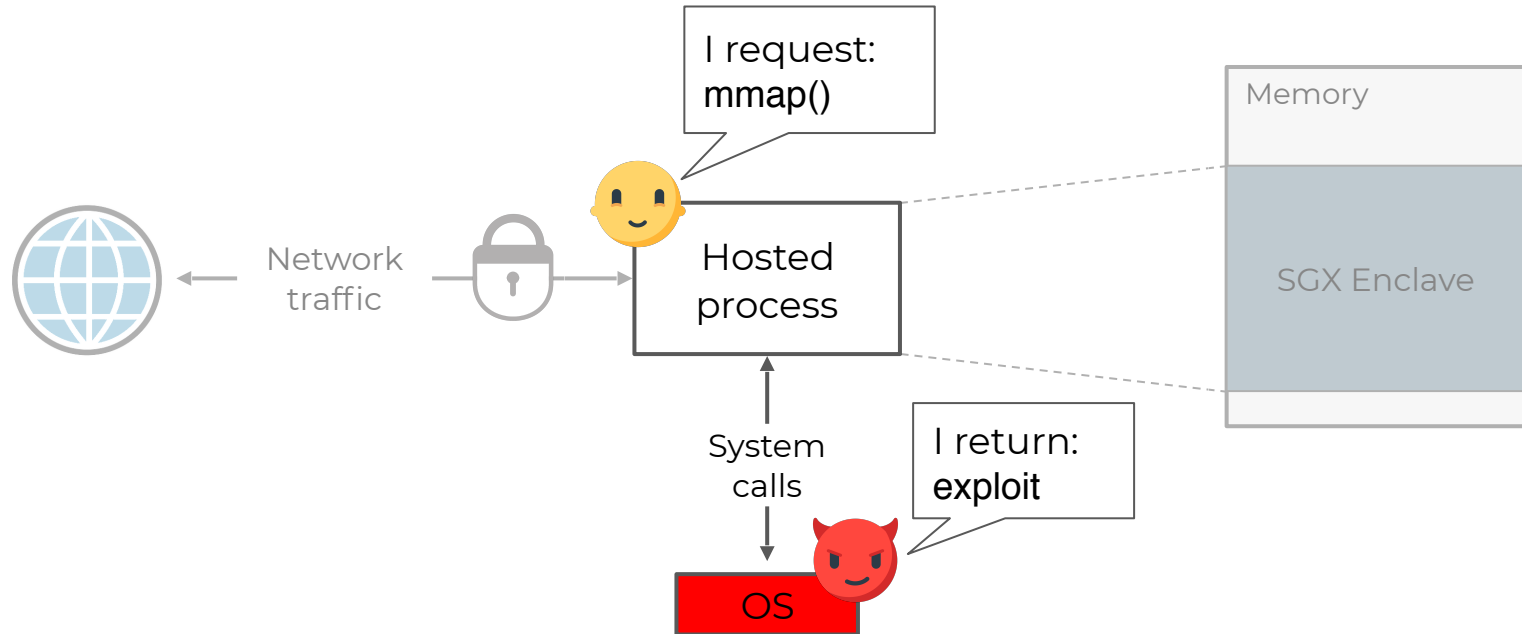
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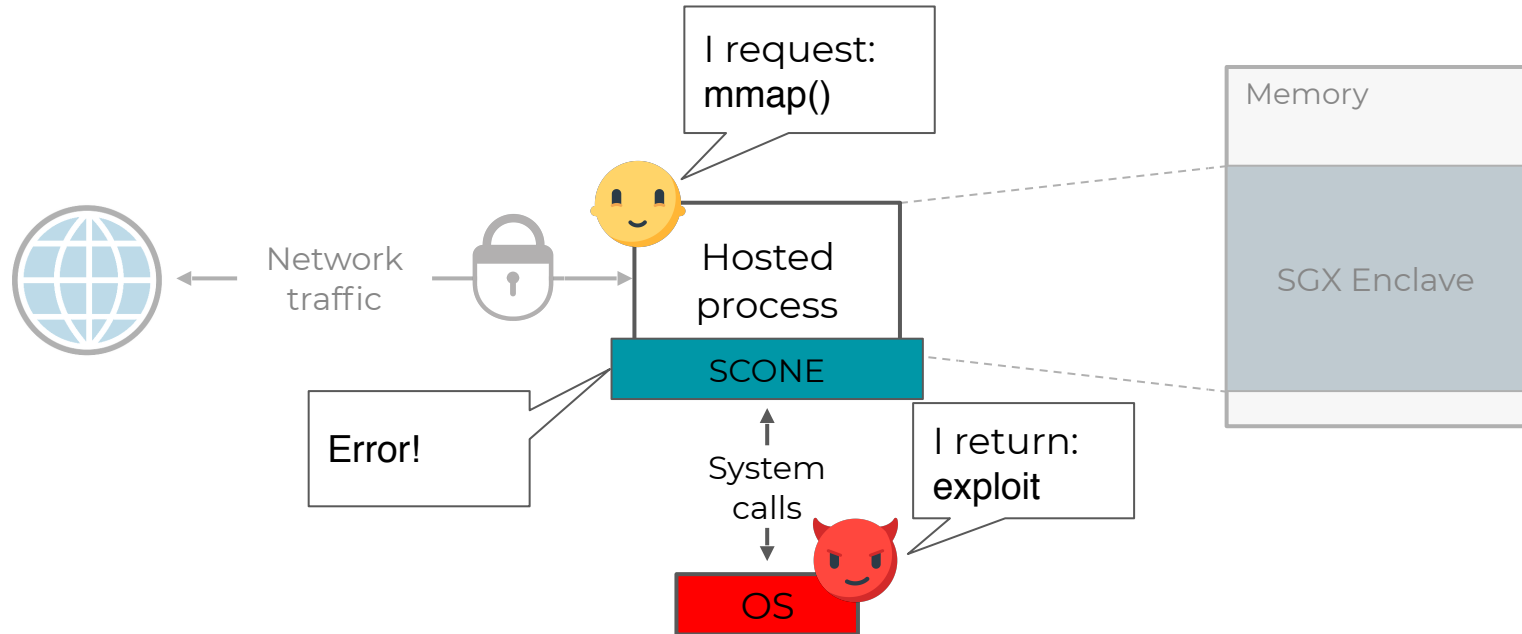
Privileged attack vectors: System Calls



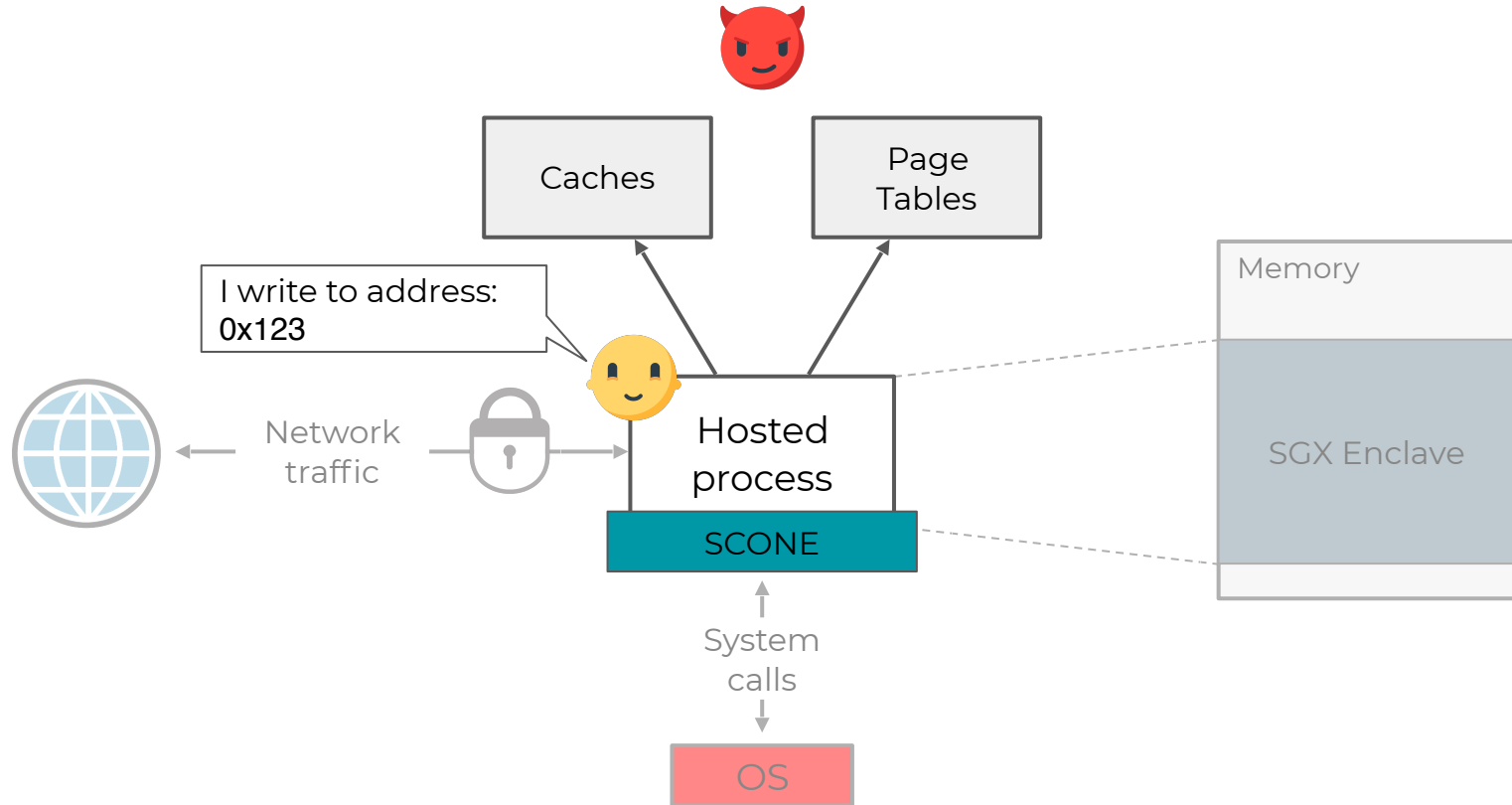
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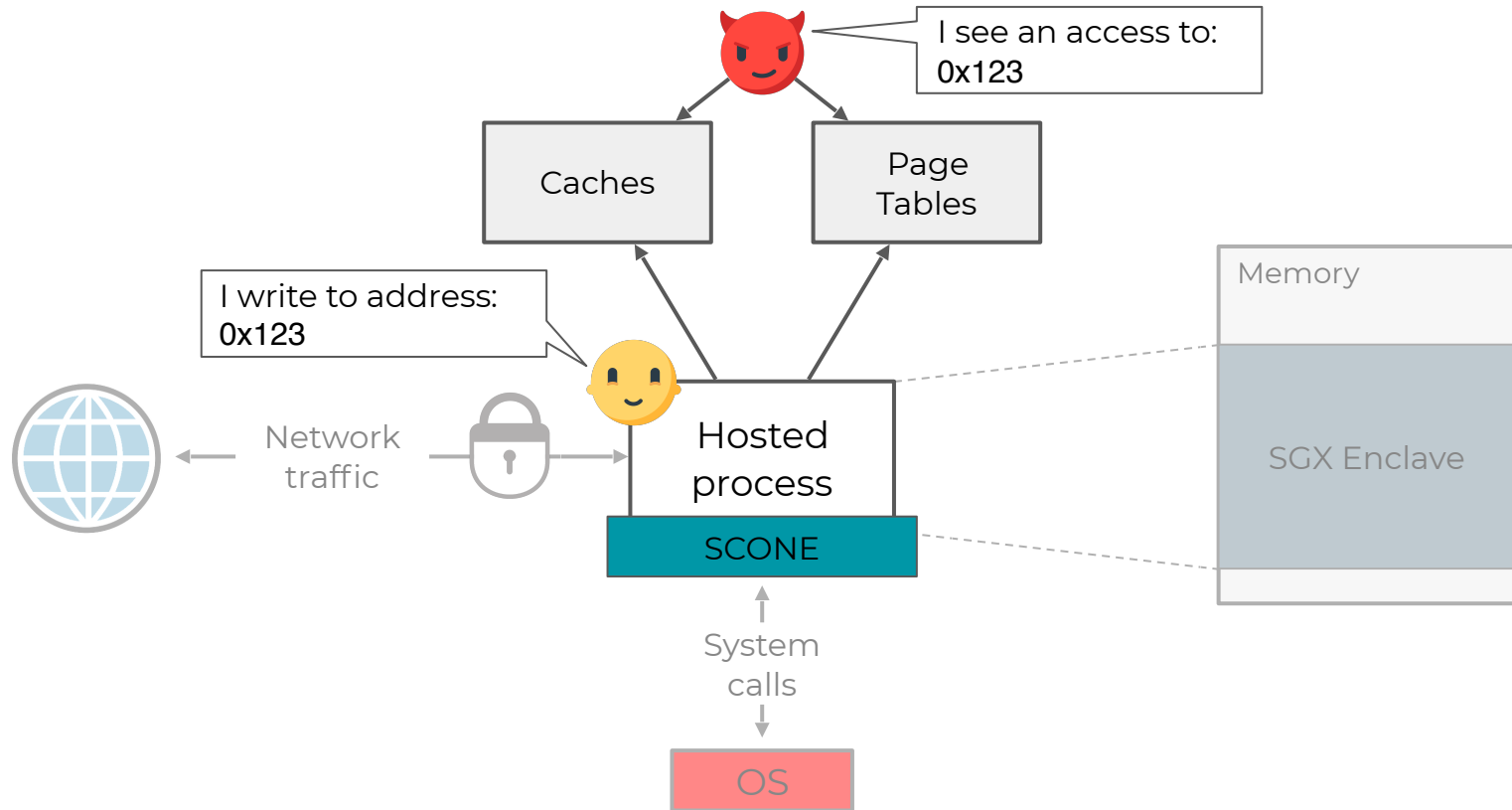
Privileged attack vectors: System Calls



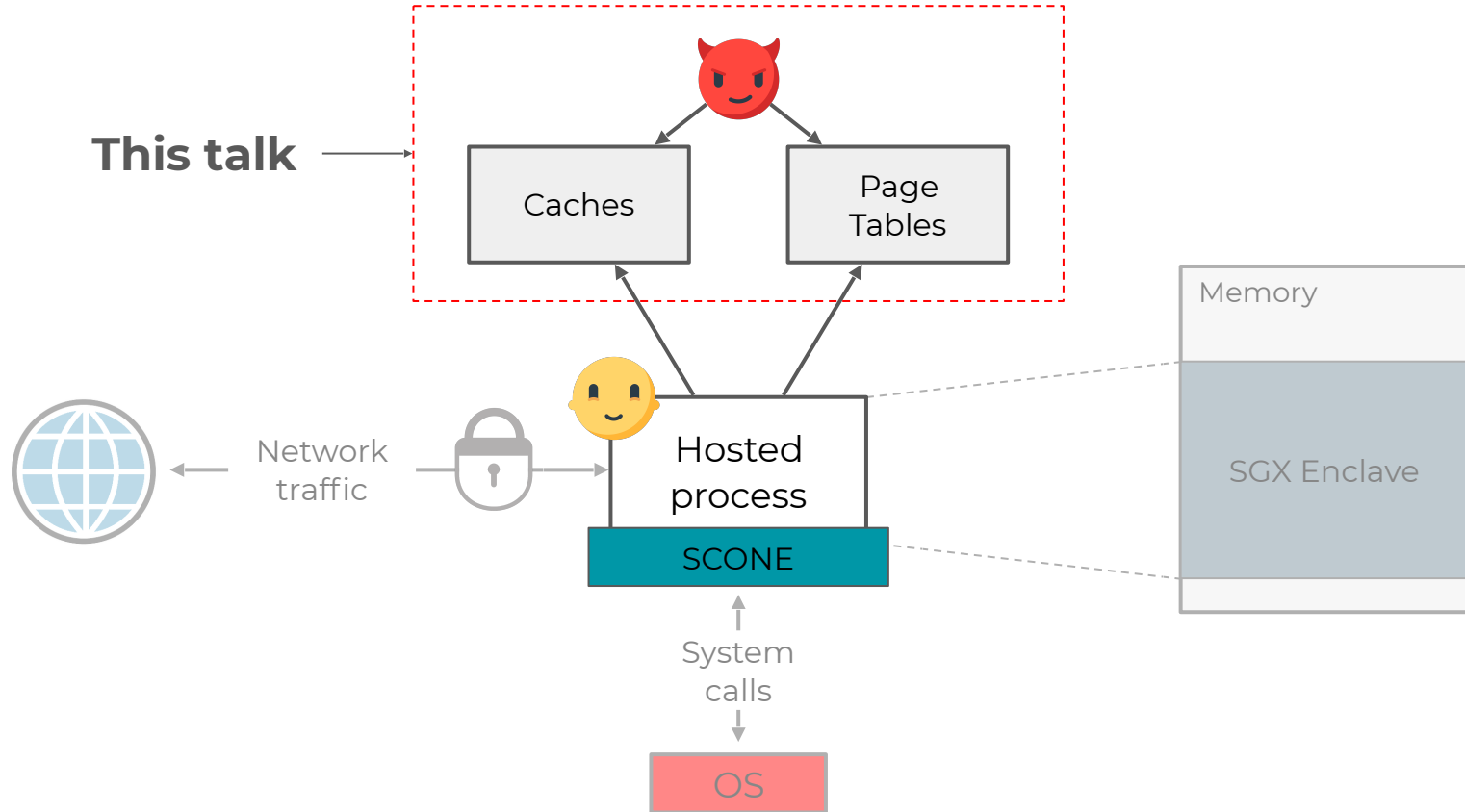
Privileged attack vectors: Shared Resources



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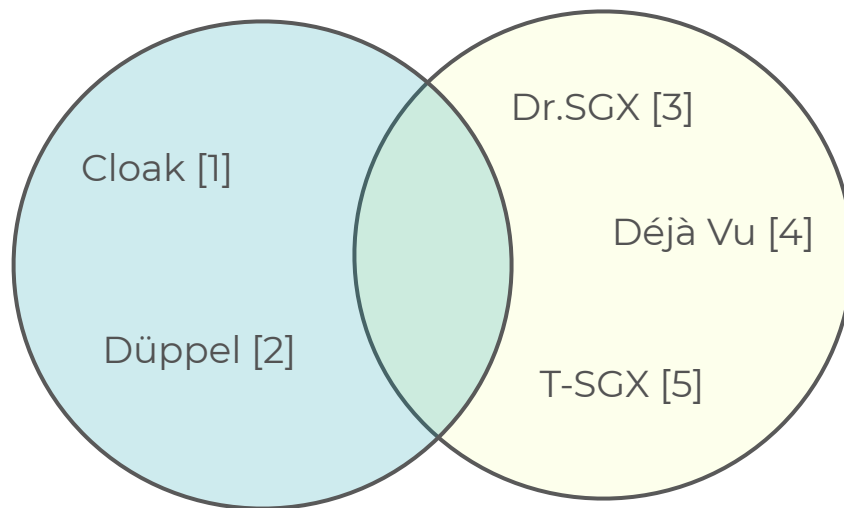


Privileged attack vectors: Shared Resources



Existing solutions

Low overhead



Low effort
(no code changes required)

[1] Gruss, D., Lettner, J., Schuster, F., Ohrimenko, O., Haller, I., & Costa, M. Strong and Efficient Cache Side-Channel Protection using Hardware Transactional Memory. In *Usenix Security 2017*.

[2] Zhang, Y., Reiter, M. K., Zhang, Y., & Reiter, M. K. Düppel: Retrofitting Commodity Operating Systems to Mitigate Cache Side Channels in the Cloud. In *CCS 2013*.

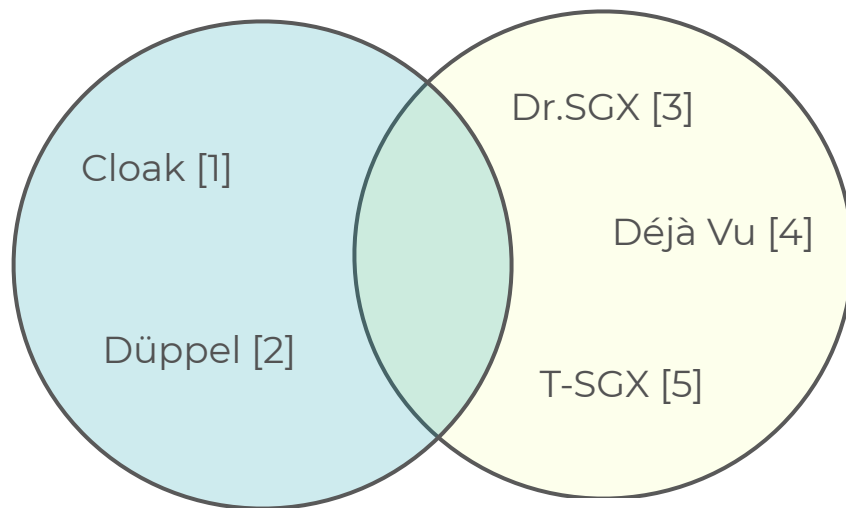
[3] Brasser, F., Capkun, S., Dmitrienko, A., Frassetto, T., Kostiaainen, K., Müller, U., & Sadeghi, A.-R. DR.SGX: Hardening SGX Enclaves against Cache Attacks with Data Location Randomization. In *arXiv 2017*.

[4] Chen, S., Reiter, M. K., Zhang, X., & Zhang, Y. Detecting Privileged Side-Channel Attacks in Shielded Execution with Déjà Vu. In *ASIA CCS '17*.

[5] Shih, M., Lee, S., & Kim, T. T-SGX: Eradicating controlled-channel attacks against enclave programs. In *NDSS 2017*.

Existing solutions

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Varys

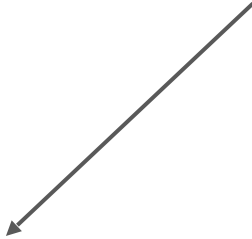
- 15% average slowdown
- No code changes

Approach

Rely but verify

Approach

Rely but verify



Request isolation from
the untrusted OS

Approach

Rely but verify

```
graph TD; A["Rely but verify"] --> B["Request isolation from the untrusted OS"]; A --> C["Check within the enclave"]
```

Request isolation from
the untrusted OS

Check within
the enclave

Complete description

Varys implements a low-cost protection for Intel SGX enclaves against side-channel attacks by creating an isolated environment and verifying it at runtime.

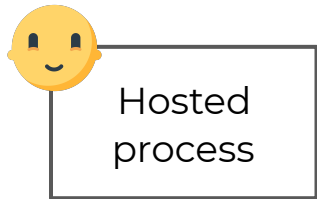
Varys implements a low-cost protection for Intel SGX enclaves against side-channel attacks by creating an isolated environment and verifying it at runtime.

Rest of the talk explains
this sentence



Varys implements a low-cost protection for Intel SGX enclaves against **side-channel attacks** by creating an isolated environment and verifying it at runtime.

Side-channel attacks



Side-channel attacks

```
if (secret == 0)
  read(addr1)
else
  read(addr2)
```



Hosted
process



Side-channel attacks

```
if (secret == 0)
  read(addr1)
else
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```



Hosted
process

Shared resource



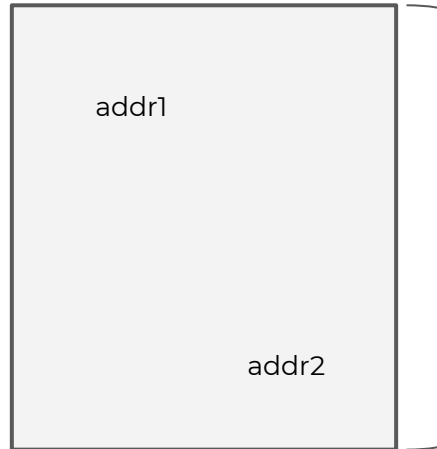
Side-channel attacks

```
if (secret == 0)
  read(addr1)
else
  read(addr2)
```



Hosted
process

Shared resource



Cleanup

Side-channel attacks

```
if (secret == 0)
  read(addr1)
else
  read(addr2)
```

Running...



Hosted
process

Shared resource



Side-channel attacks

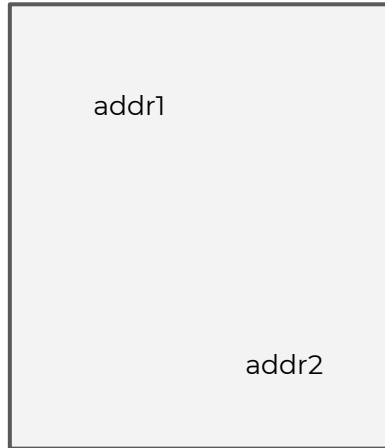
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Running...



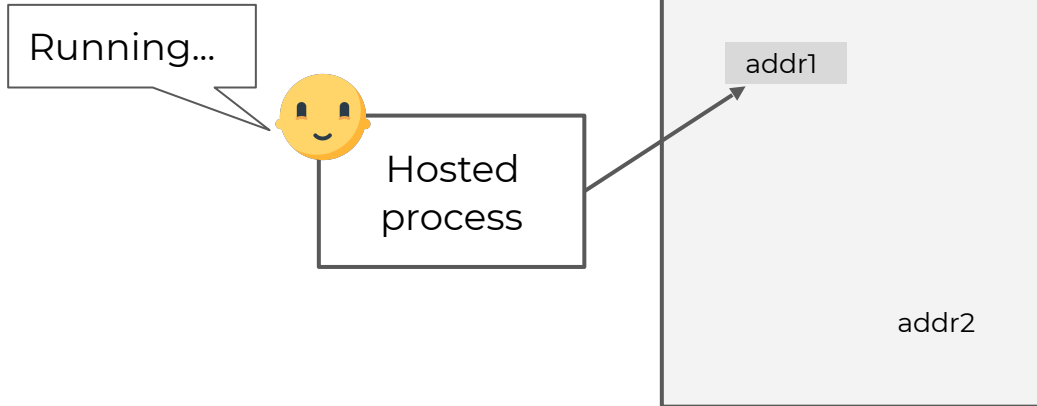
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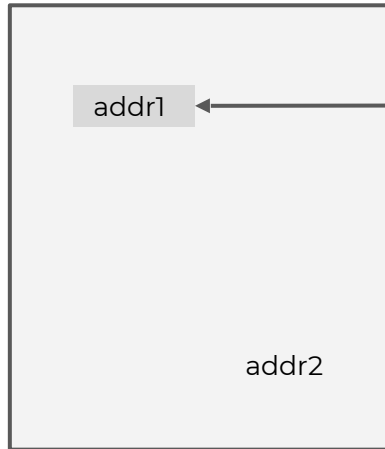
Side-channel attacks

```
if (secret == 0)
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else
  read(addr2)
```



Hosted
process

Shared resource



addr1 was
accessed!

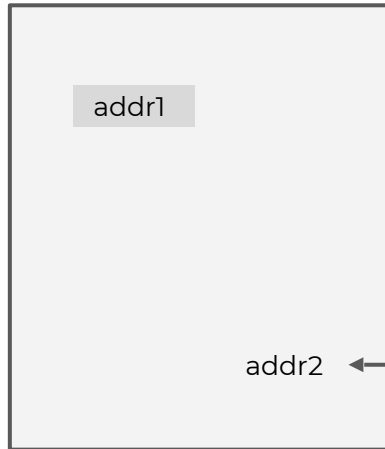
Side-channel attacks

```
if (secret == 0)
  read(addr1)
else
  read(addr2)
```



Hosted
process

Shared resource



addr2



addr2 was not
accessed!

Side-channel attacks



Side-channel attacks



Vulnerable shared resources

- CPU caches
- Page tables
- FPU
- Memory bus
- ...



Laura Abbott
@openiabbott

Follow

slaps modern cpu You won't believe how many side channels this thing can hold

7:44 AM - 10 Jul 2018

Vulnerable shared resources

- CPU caches (L1, L2)
 - Page tables
 - FPU
 - Memory bus
 - ...
- } **Varys**



Laura Abbott
@openiabbott

Follow

slaps modern cpu You won't believe how many side channels this thing can hold

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Varys implements a low-cost protection for Intel SGX enclaves against side-channel attacks by creating an **isolated environment** and verifying it at runtime.

Attack requirements




- High interrupt rate
- Predefined cache state
- Shared core

Attack requirements




- ~~High interrupt rate~~
 - ~~Predefined cache state~~
 - ~~Shared core~~
- } Isolated environment

Varys implements a low-cost protection for Intel SGX enclaves against side-channel attacks by **creating** an isolated environment and **verifying it at runtime**.

Design

- High preemption rate  Restrict and terminate
- Predefined cache state  Cache eviction
- Shared core  Trusted reservation

Design

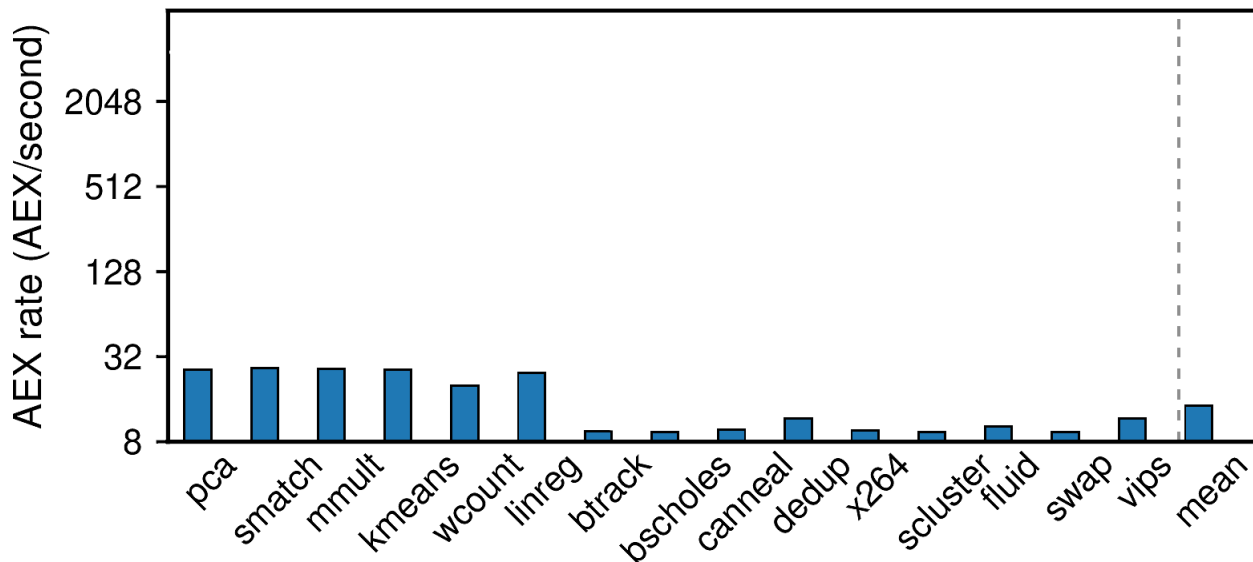
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Restricting preemption rate

- Attack exit rate: ~ 5000 exits/s.

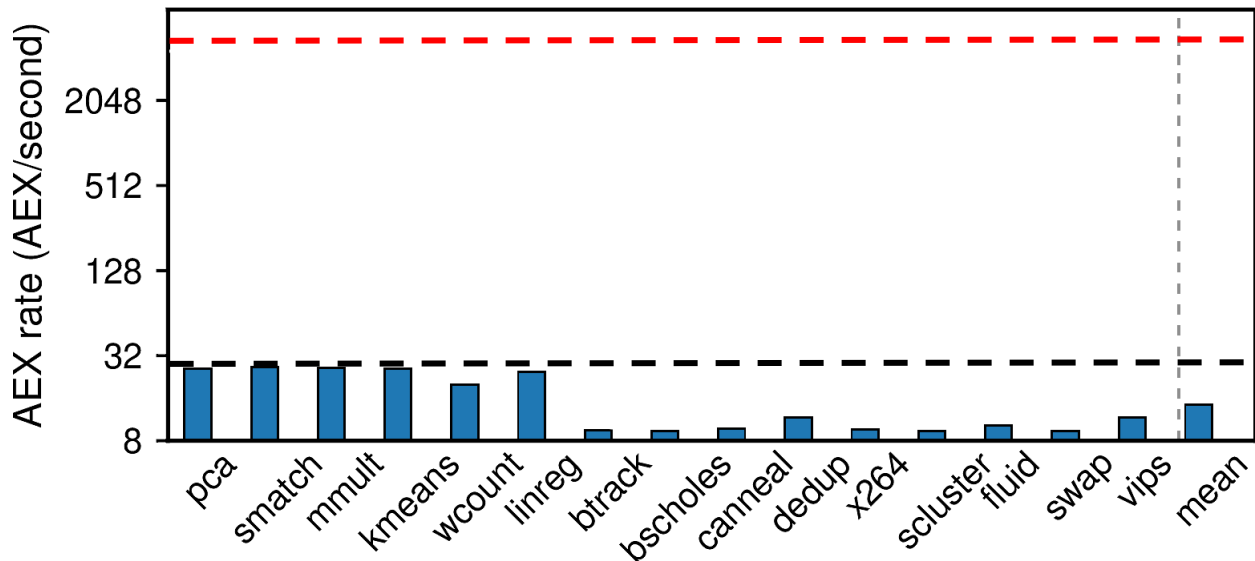
Restricting preemption rate

- Attack exit rate: ~ 5000 exits/s.
- Normal exit rate: ~ 30 exits/s.

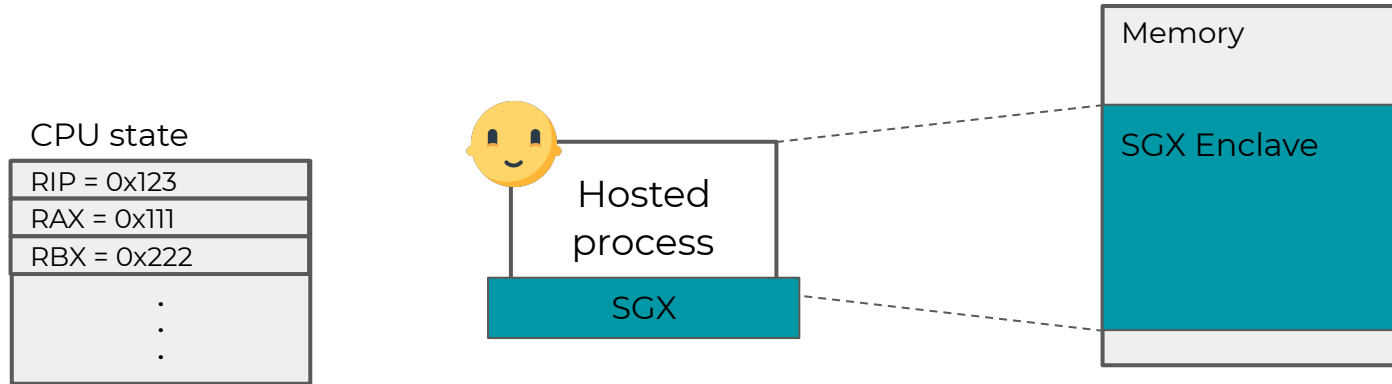


Restricting preemption rate

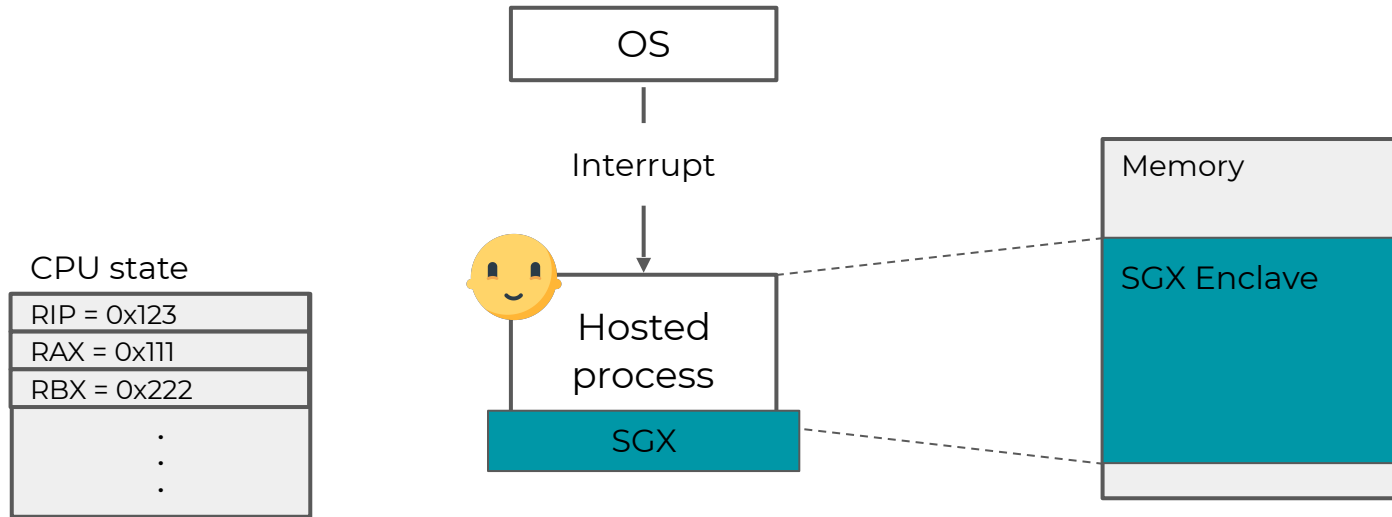
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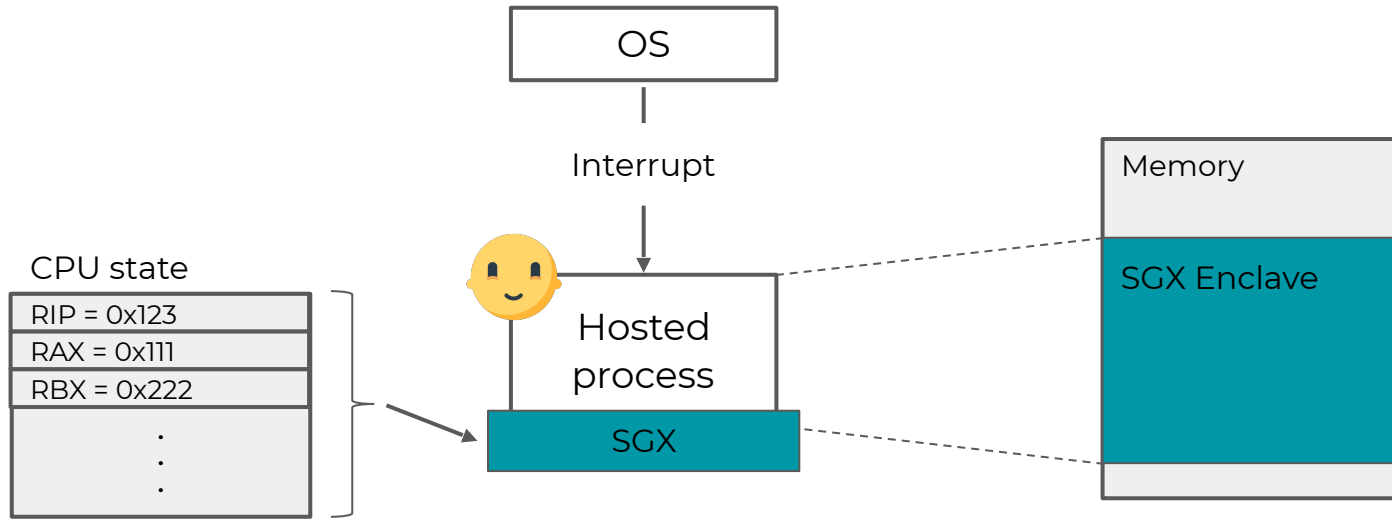
Asynchronous Enclave Exit (AEX)



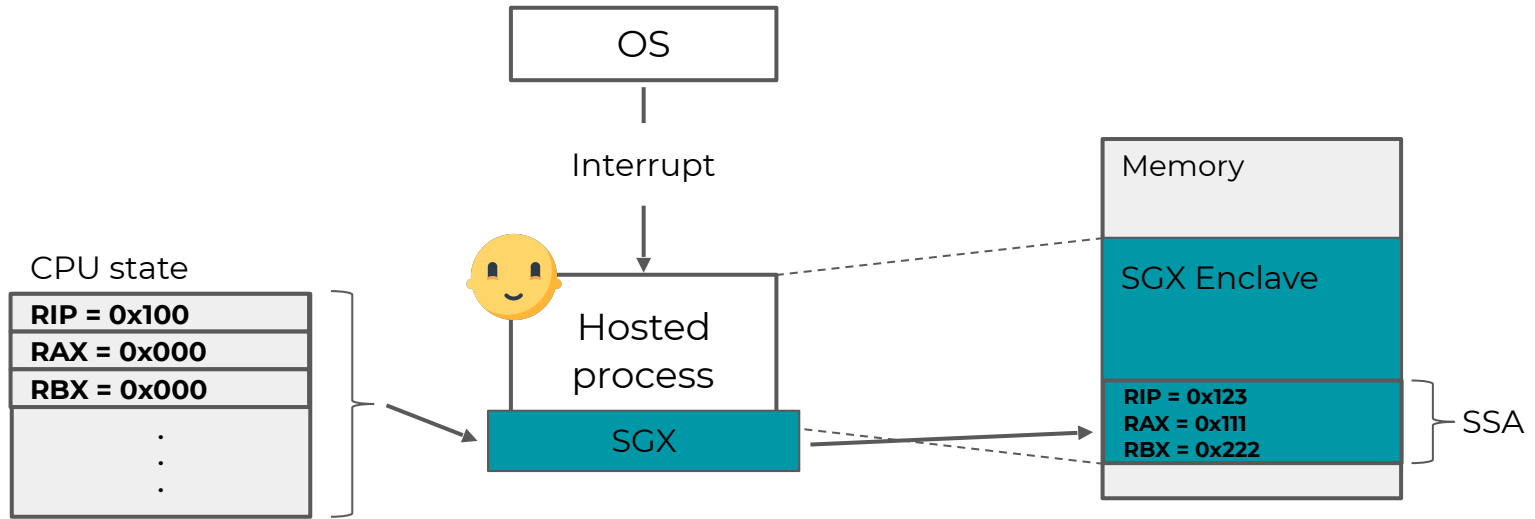
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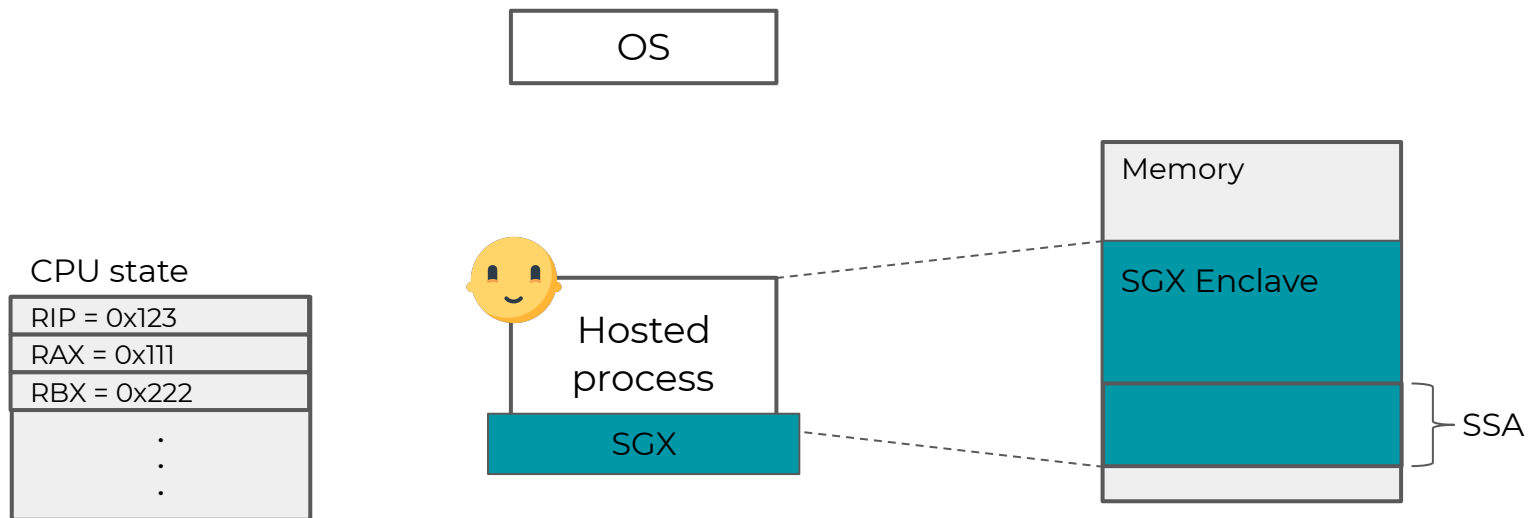
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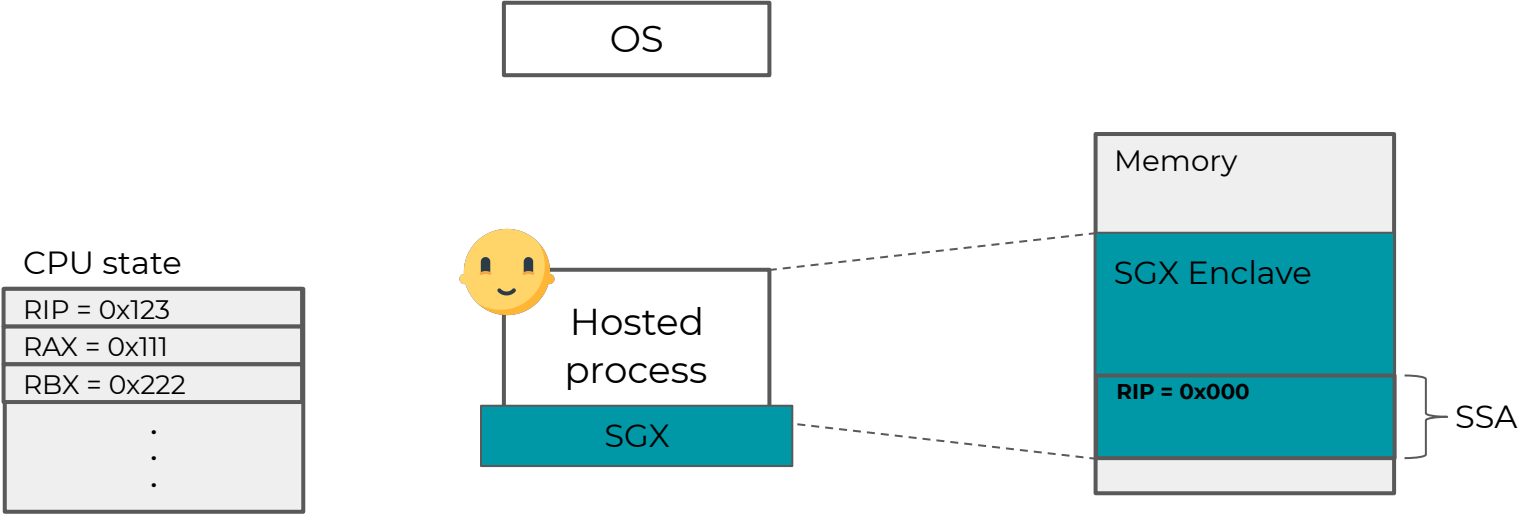
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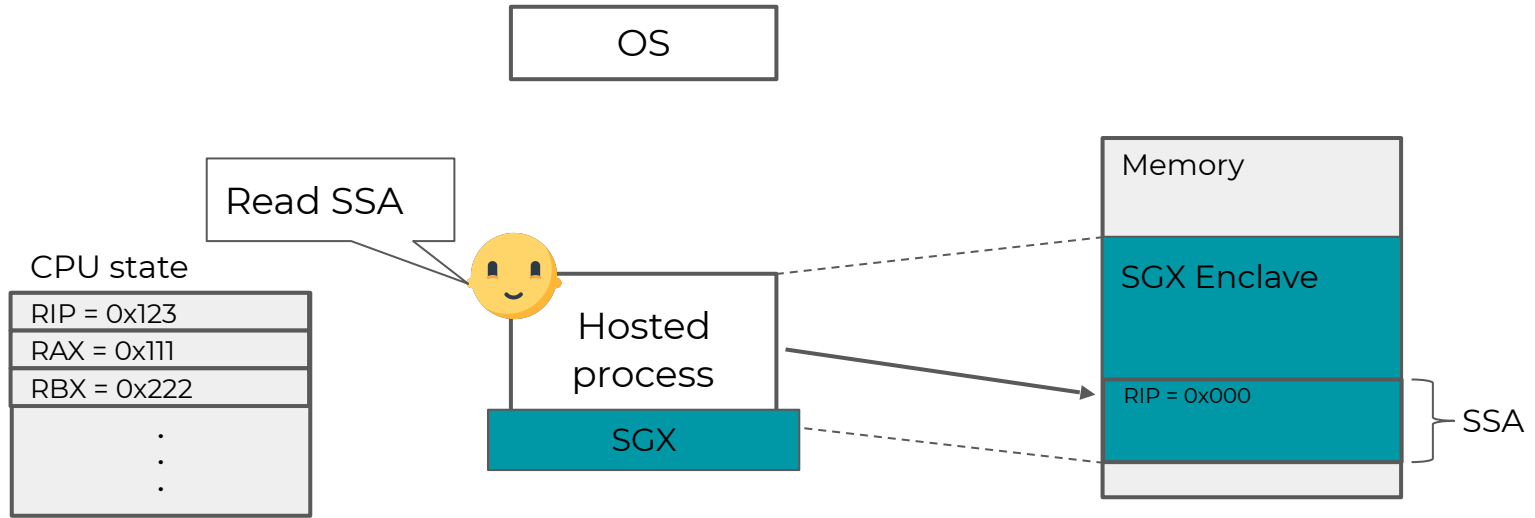
Detecting interrupts



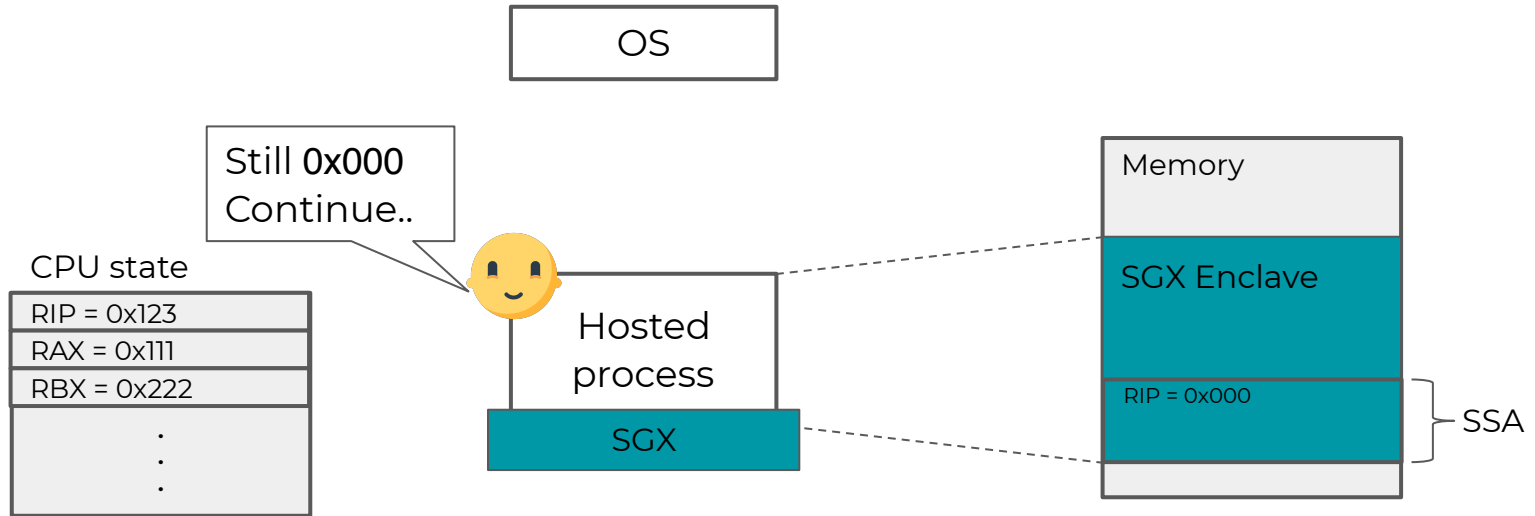
Detecting interrupts



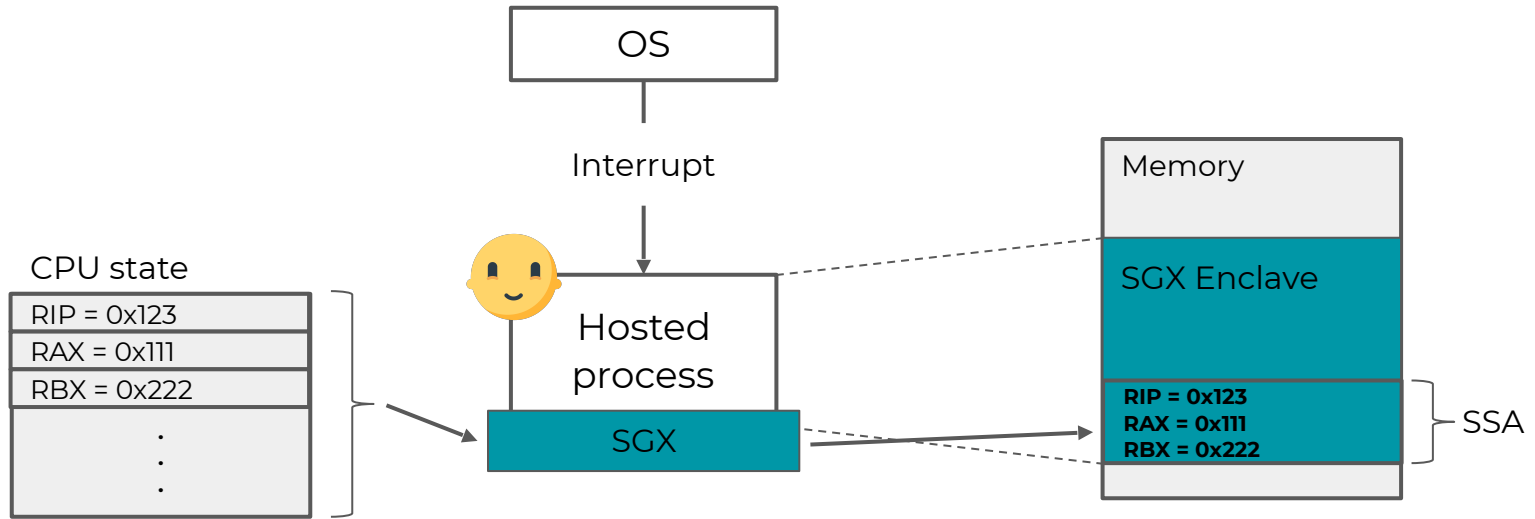
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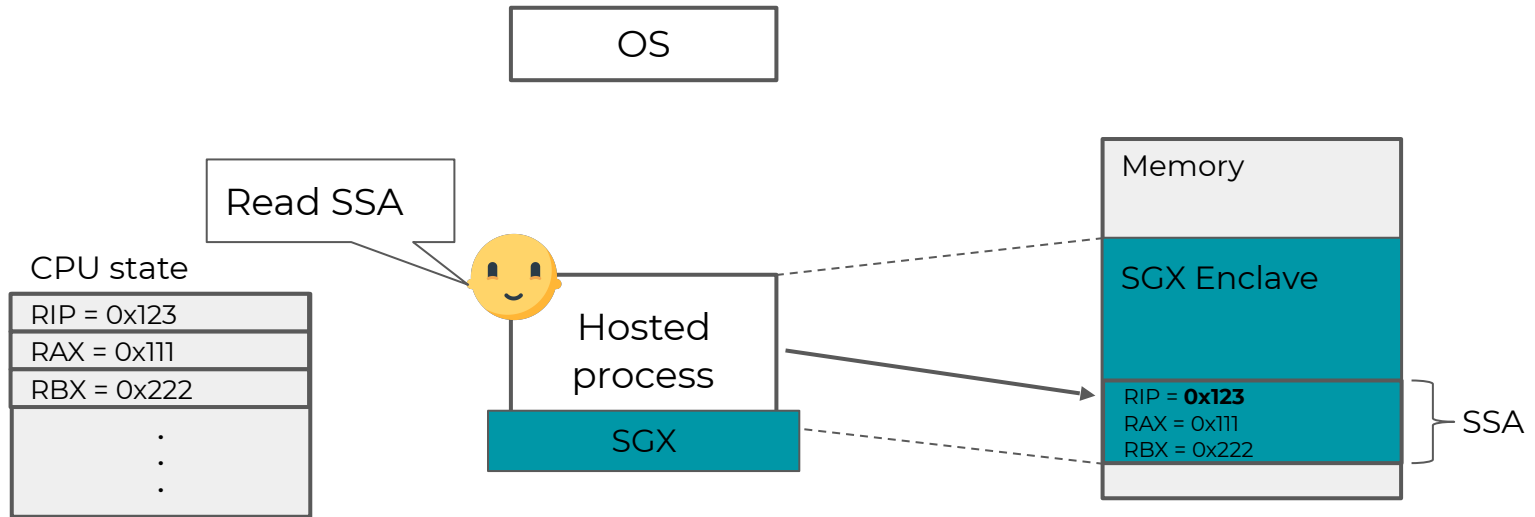
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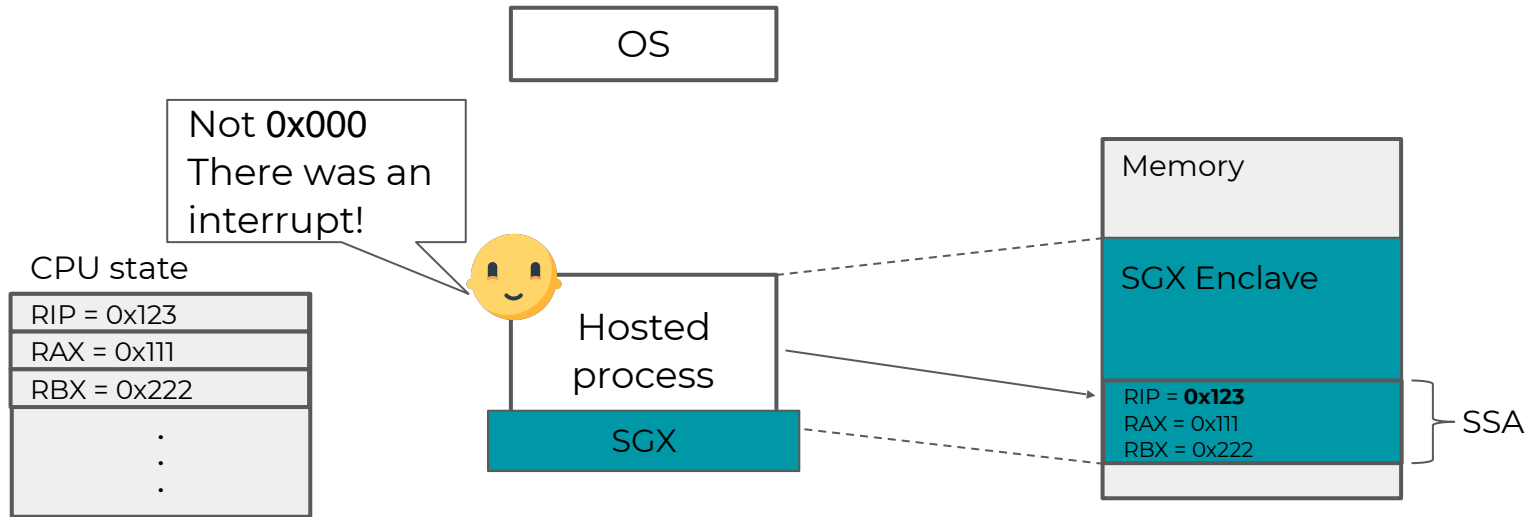
Detecting interrupts






Detecting interrupts



Detecting interrupts



Design

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Hiding cache traces

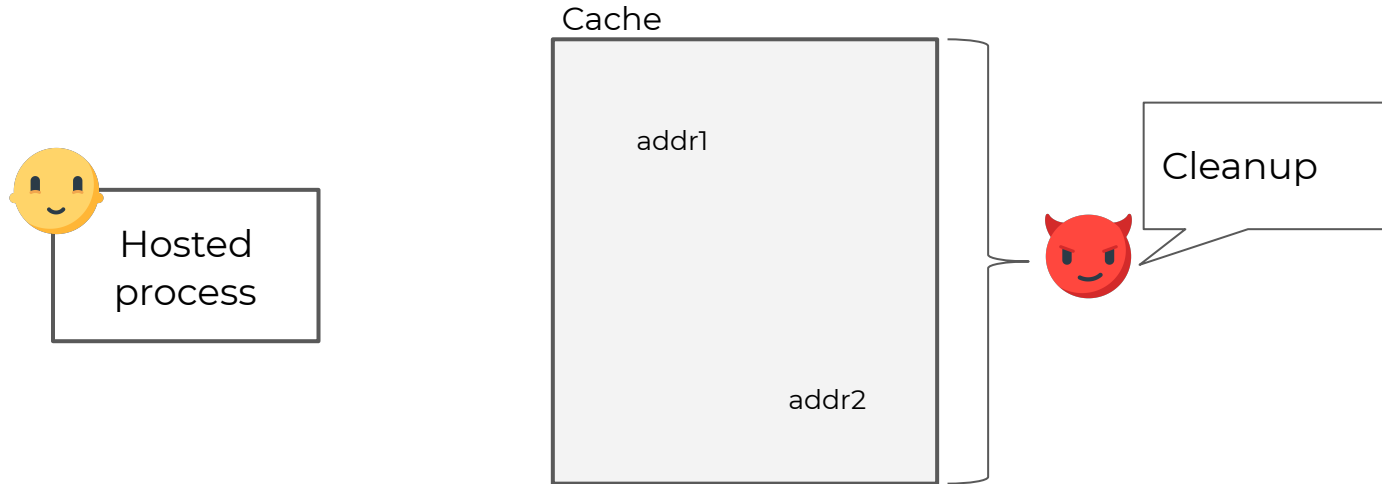


Hosted
process

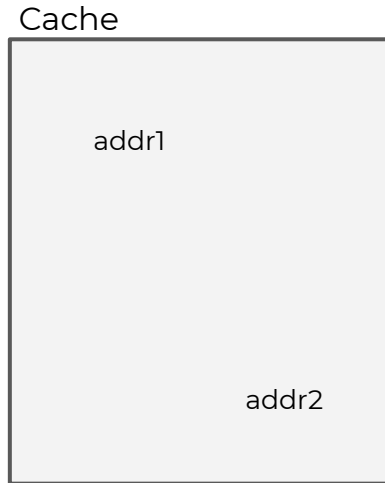
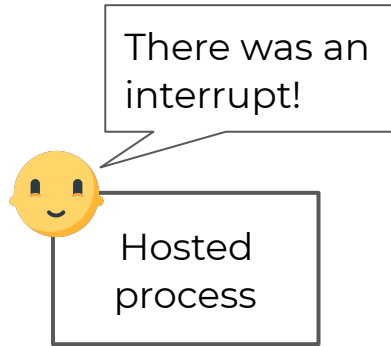
Cache



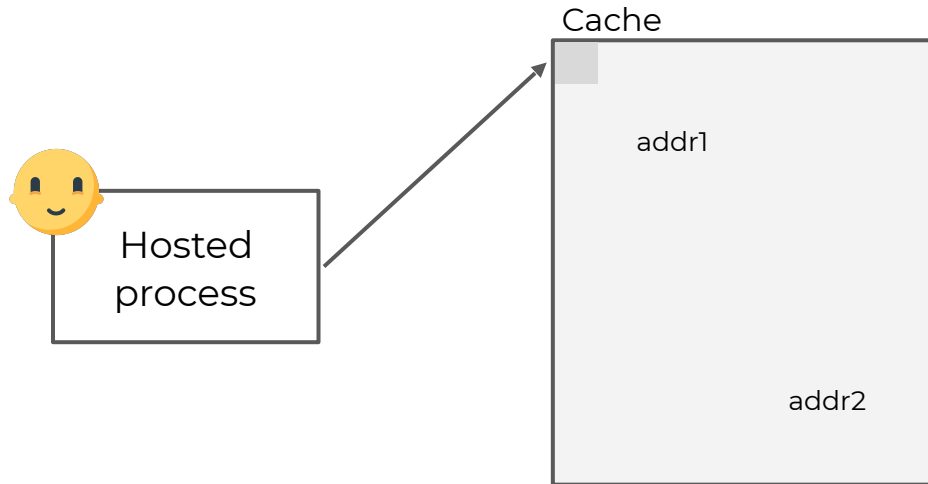
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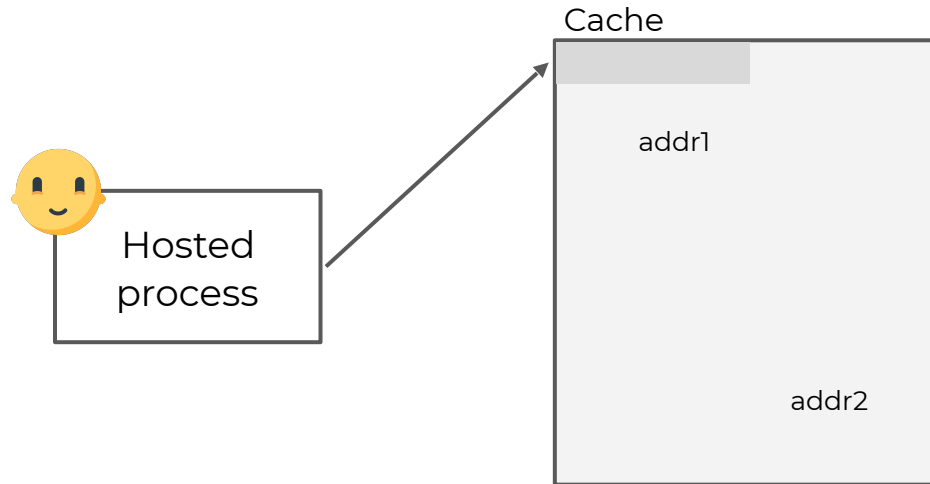
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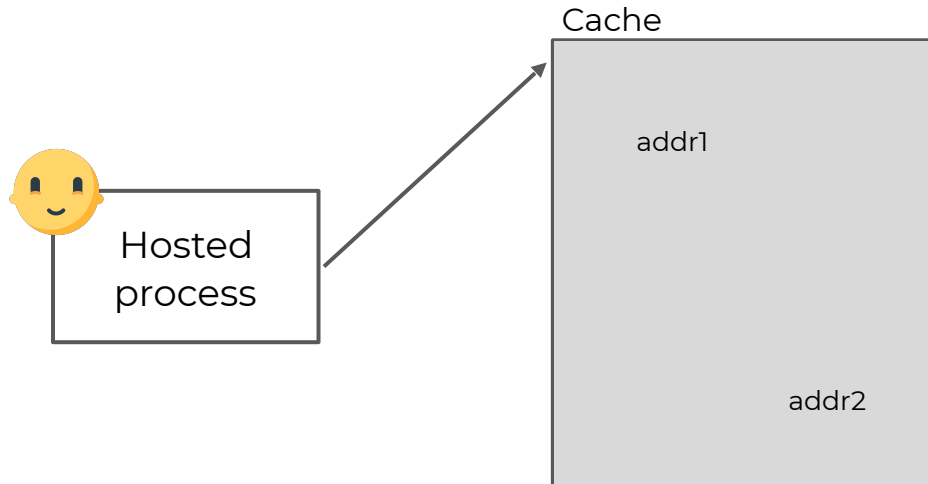
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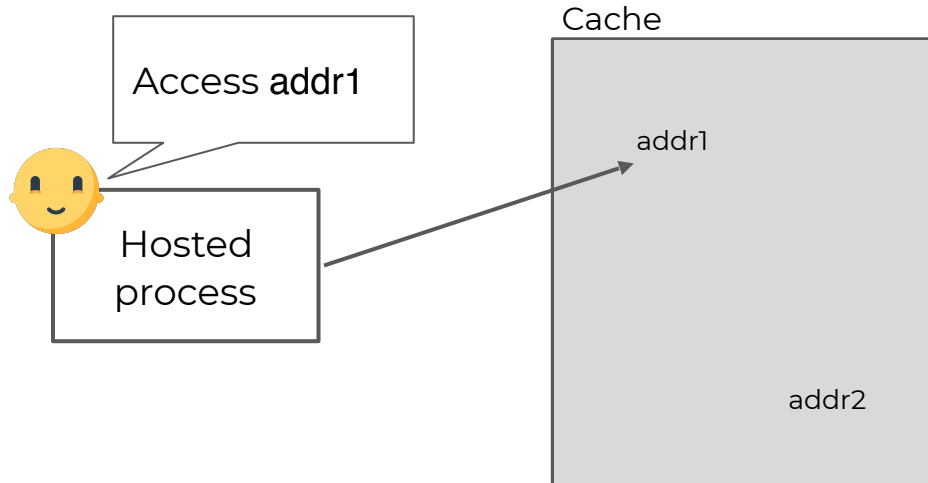
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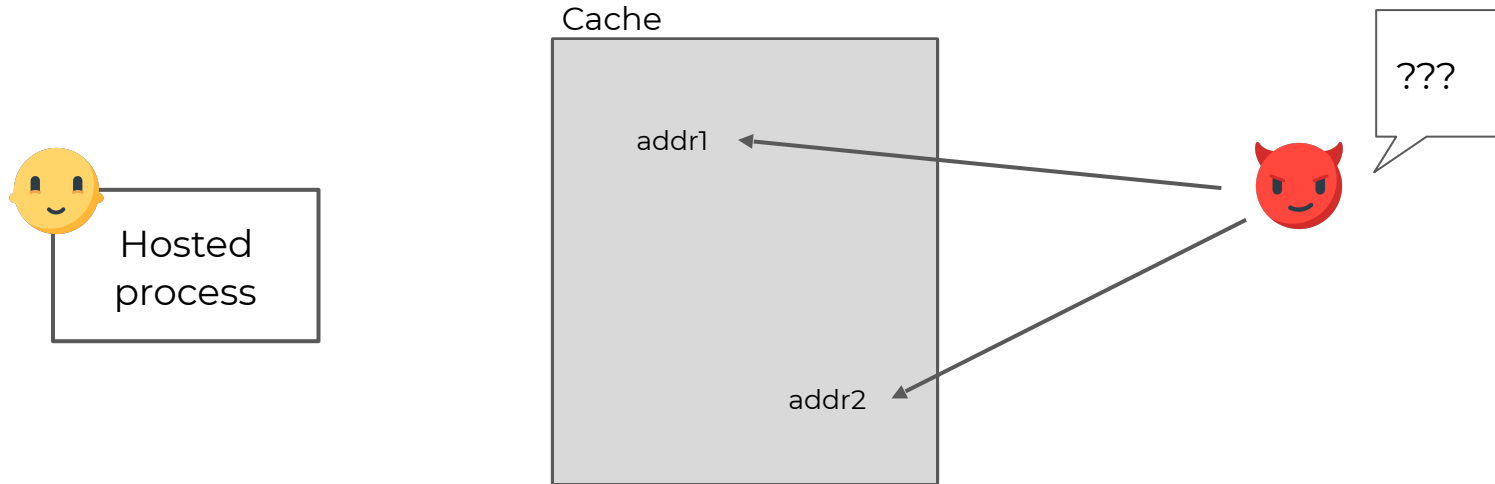
Hiding cache traces






Hiding cache traces



Hiding cache traces

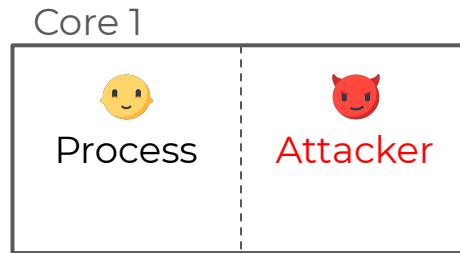


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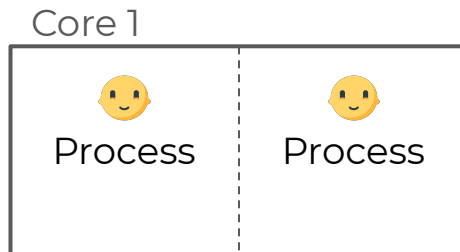
Preventing core sharing

- Occupy both hyperthreads



Preventing core sharing

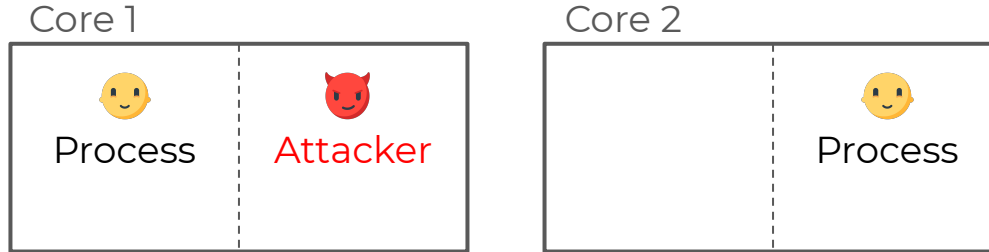
- Occupy both hyperthreads
 - Use process affinity



How do we ensure reservation?

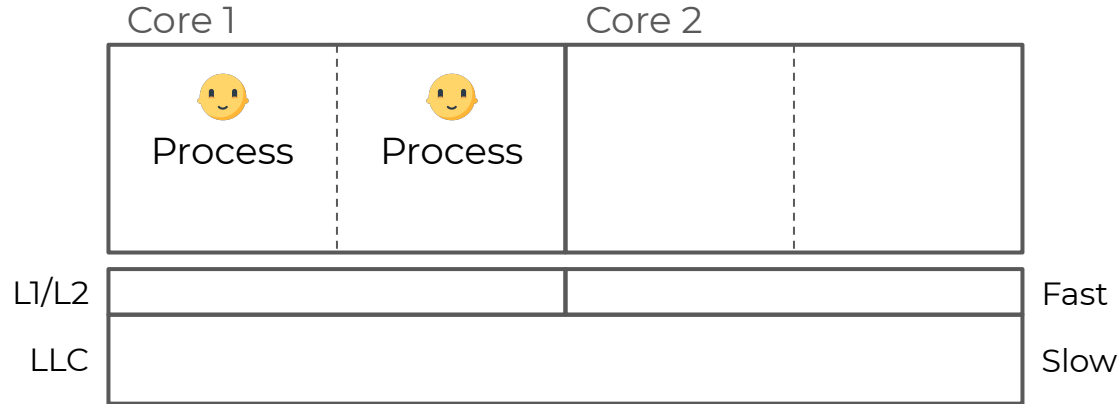


How do we ensure reservation?



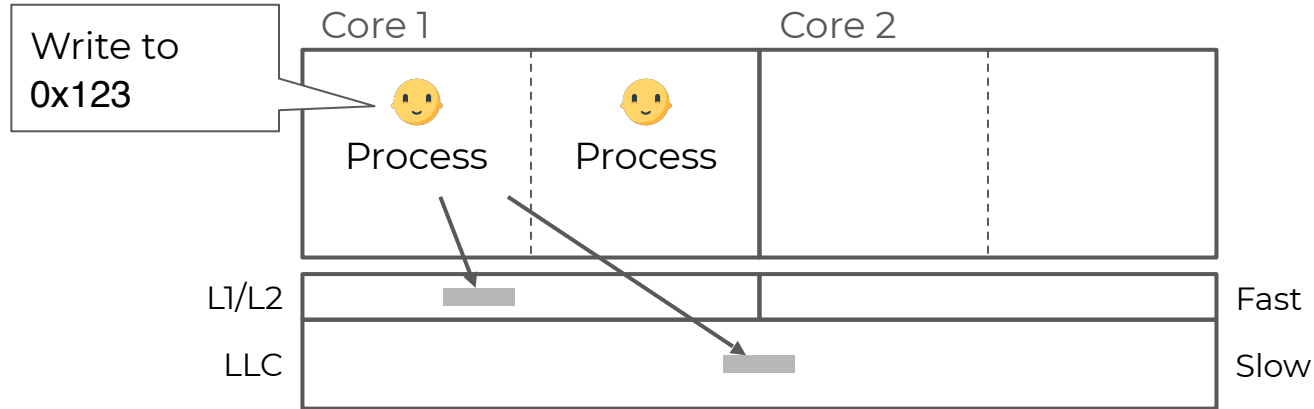
Handshake

- Use shared access timing



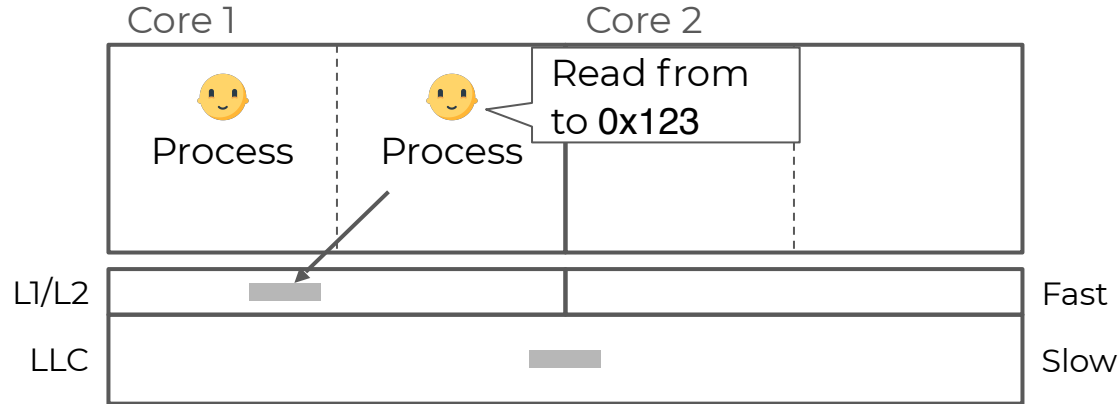
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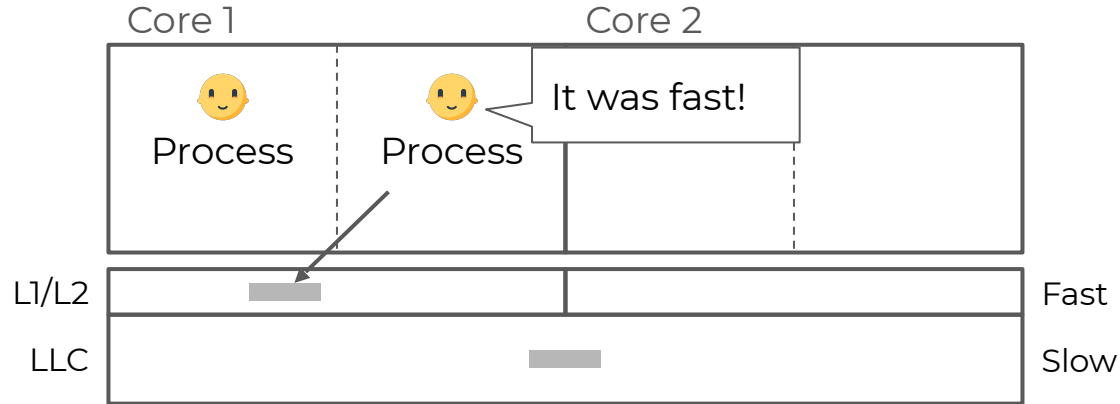
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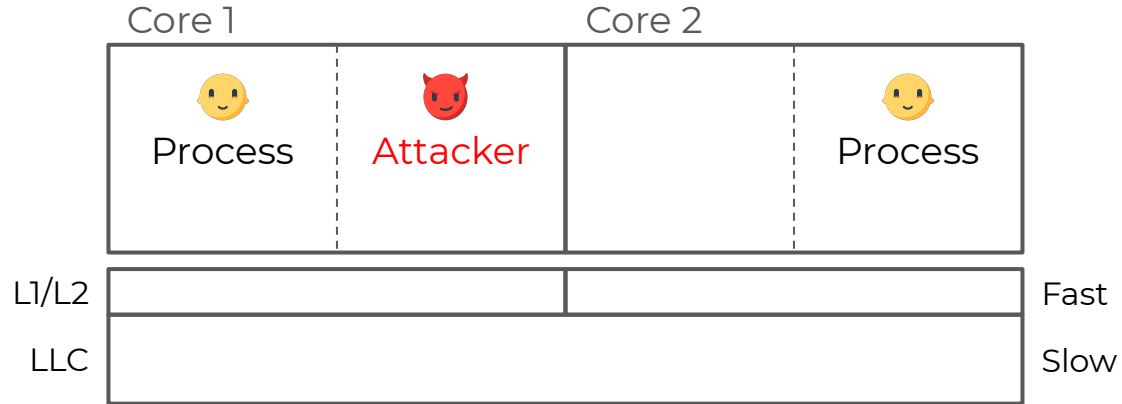
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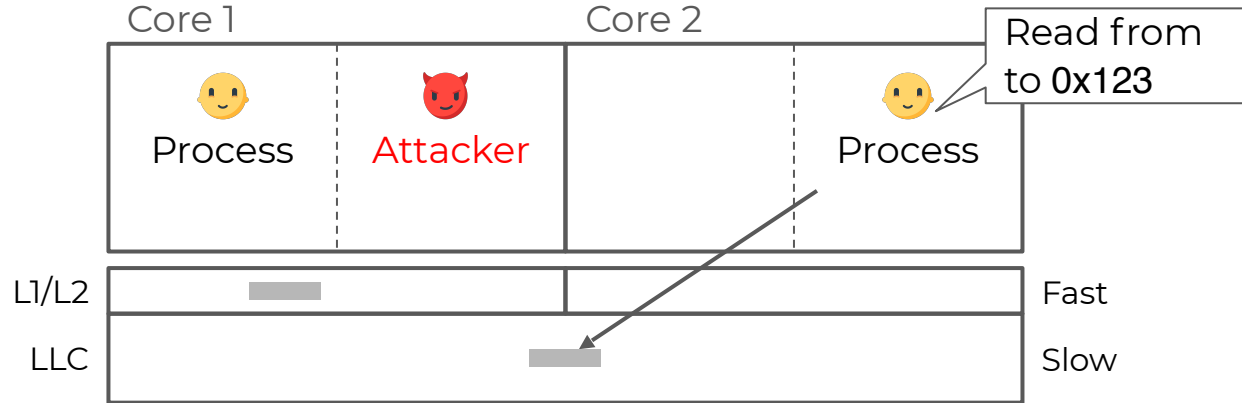
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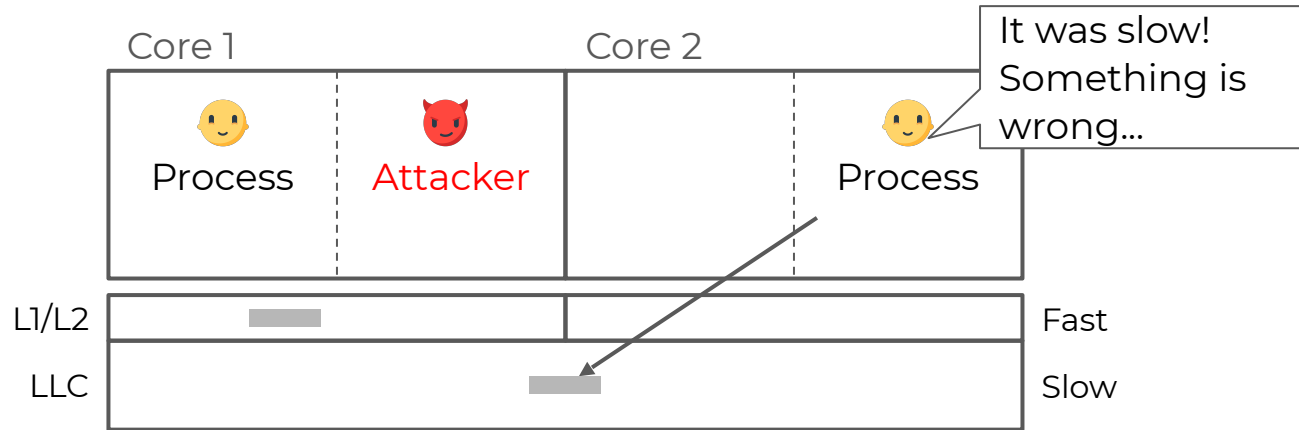
Handshake

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Handshake

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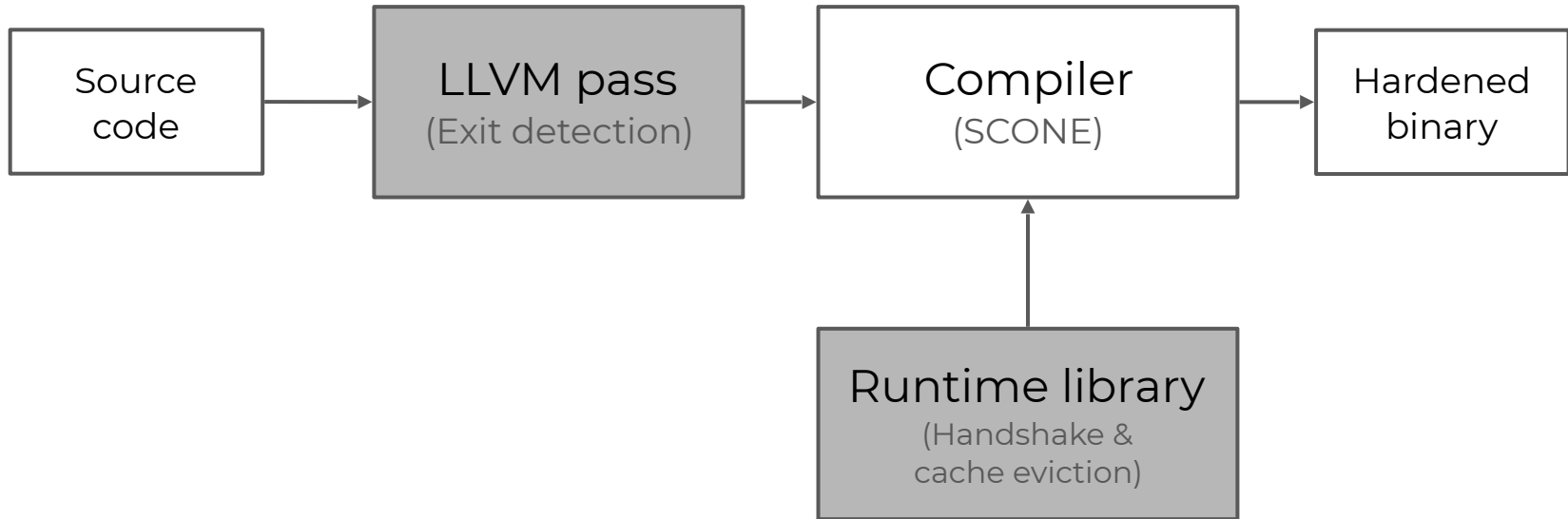


Design

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- Shared core  Trusted reservation

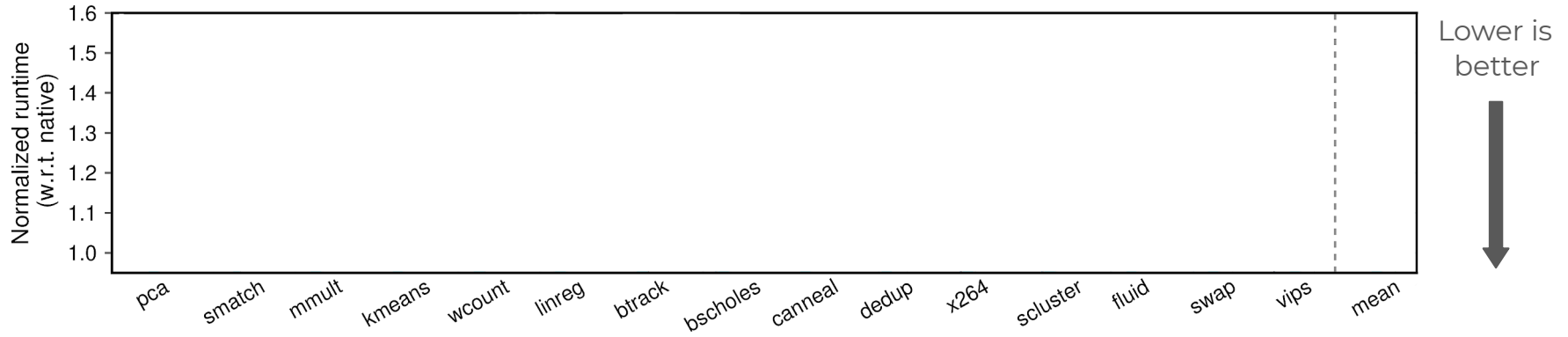
Varys **implements** a low-cost protection for Intel SGX enclaves against side-channel attacks by creating an isolated environment and verifying it at runtime.

Implementation

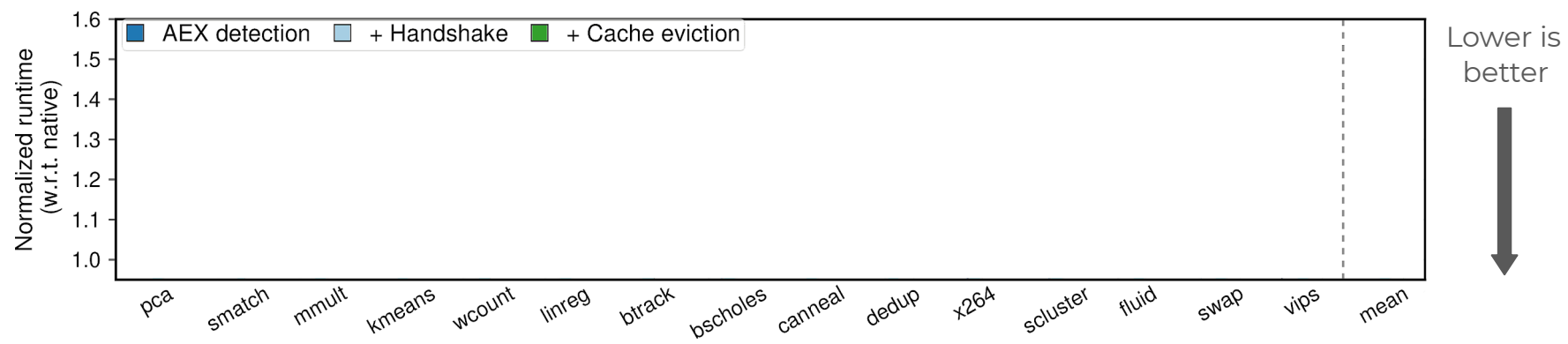


Varys implements a **low-cost** protection for Intel SGX enclaves against side-channel attacks by creating an isolated environment and verifying it at runtime.

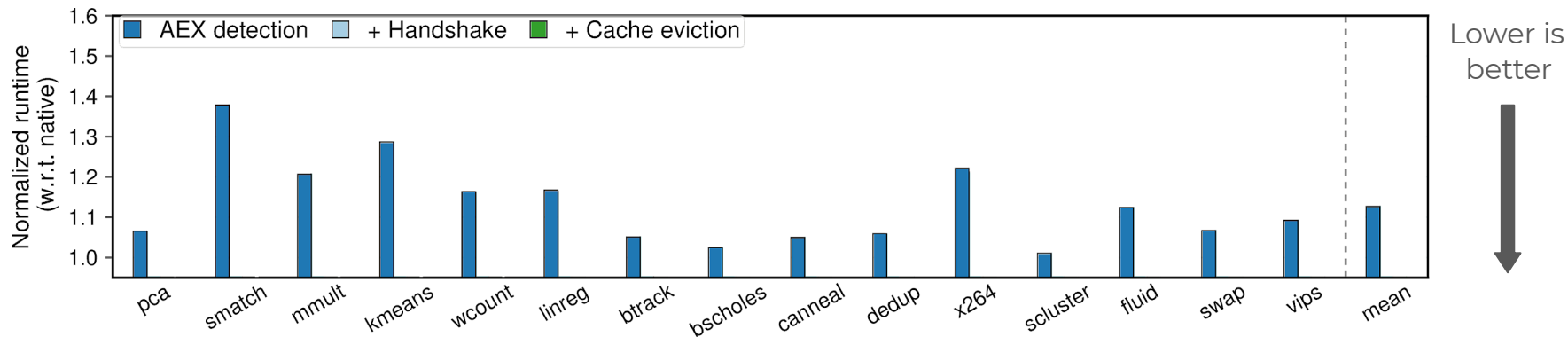
Evaluation: performance



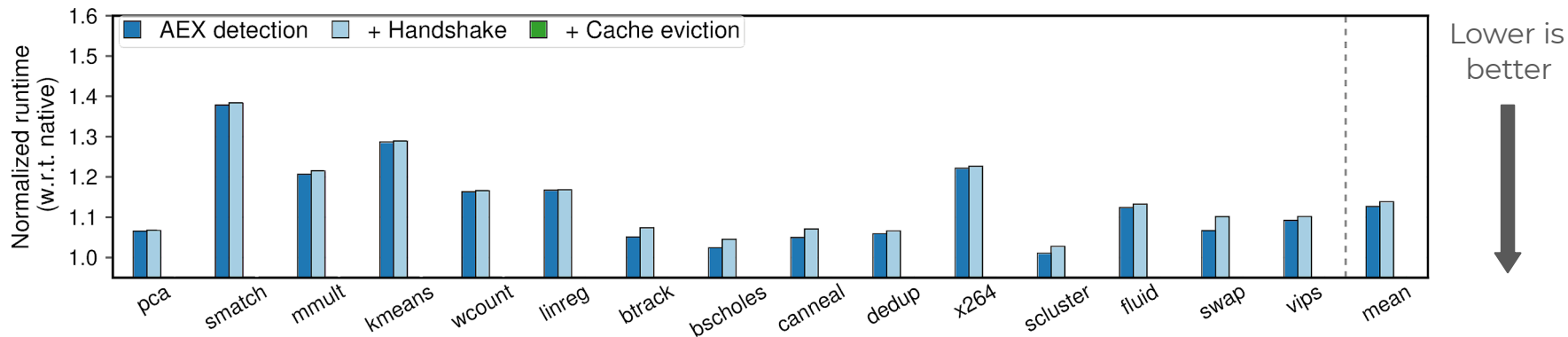
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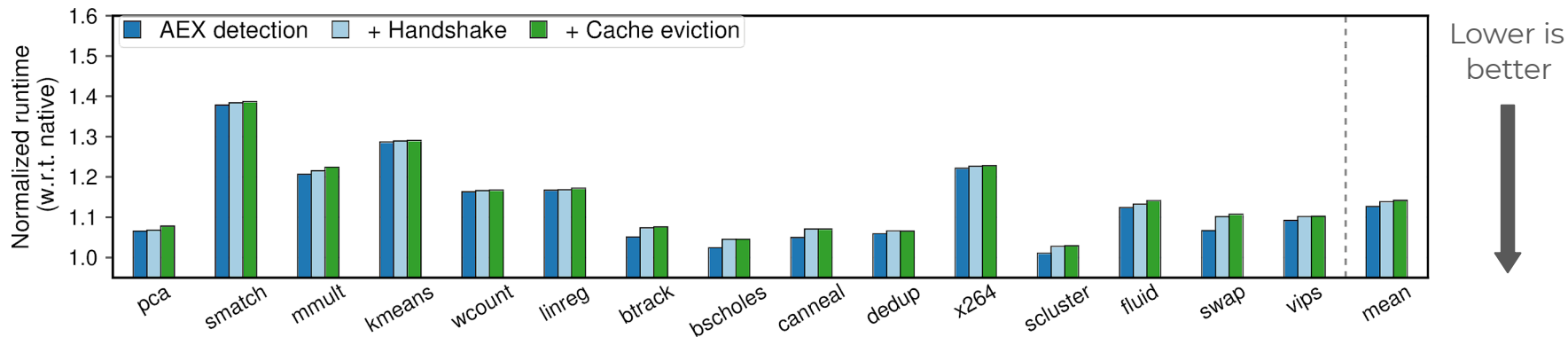
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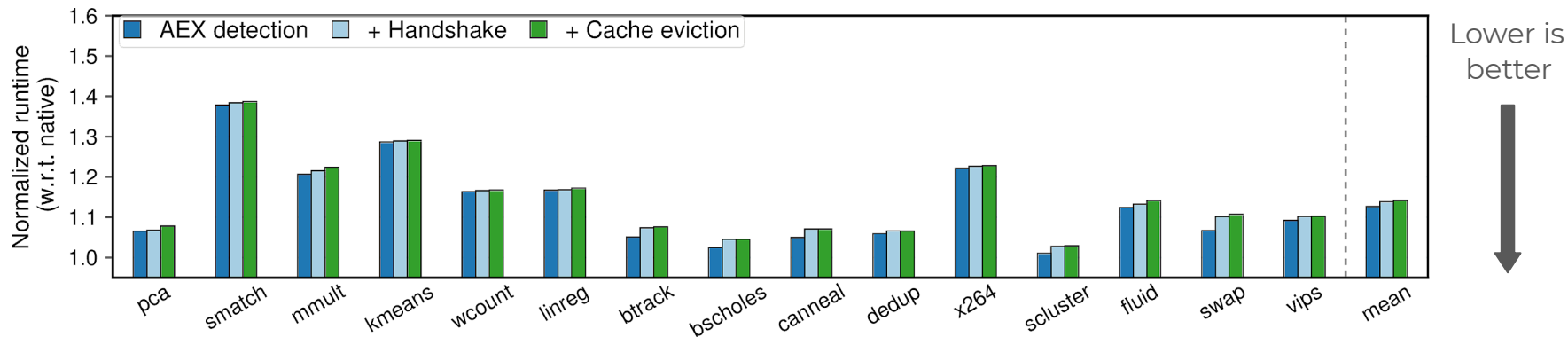
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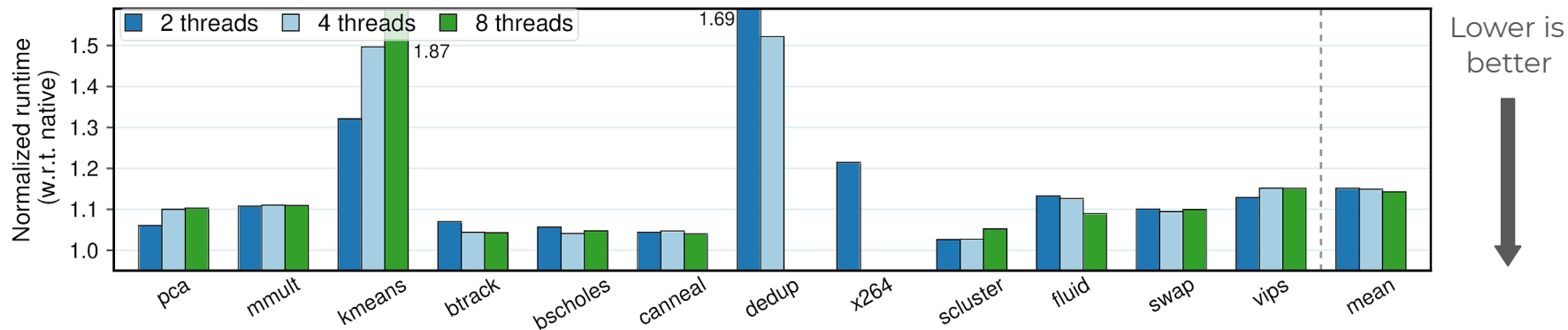


Handshake and eviction **only at enclave exits**

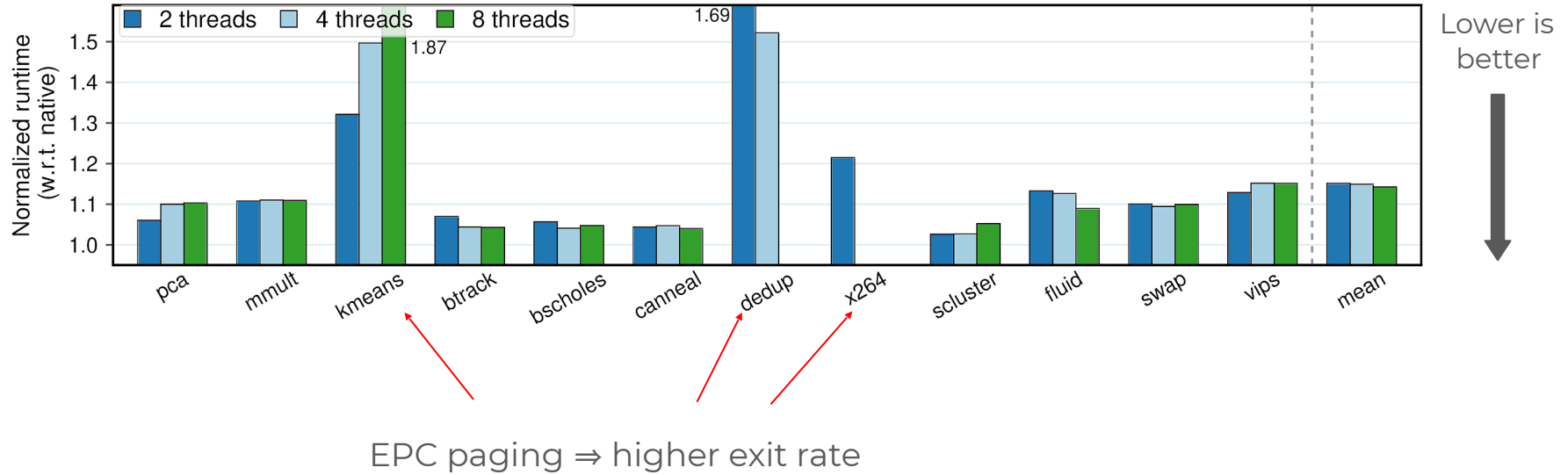
- 20-30 times per second

Evaluation: multithreading

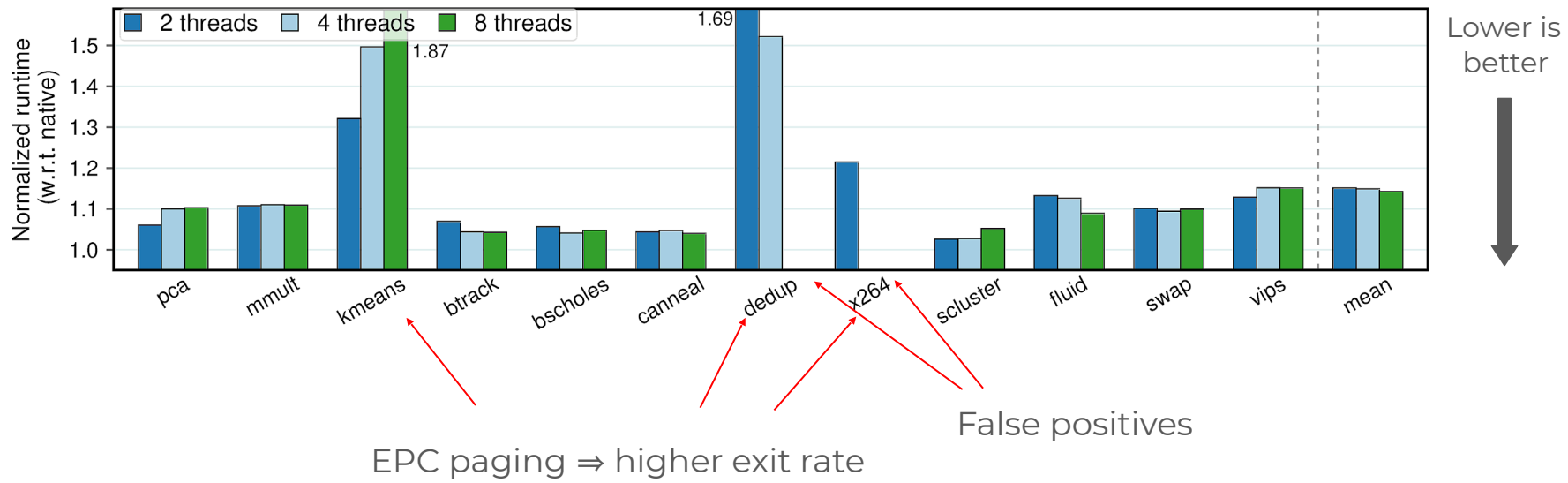
Evaluation: multithreading



Evaluation: multithreading



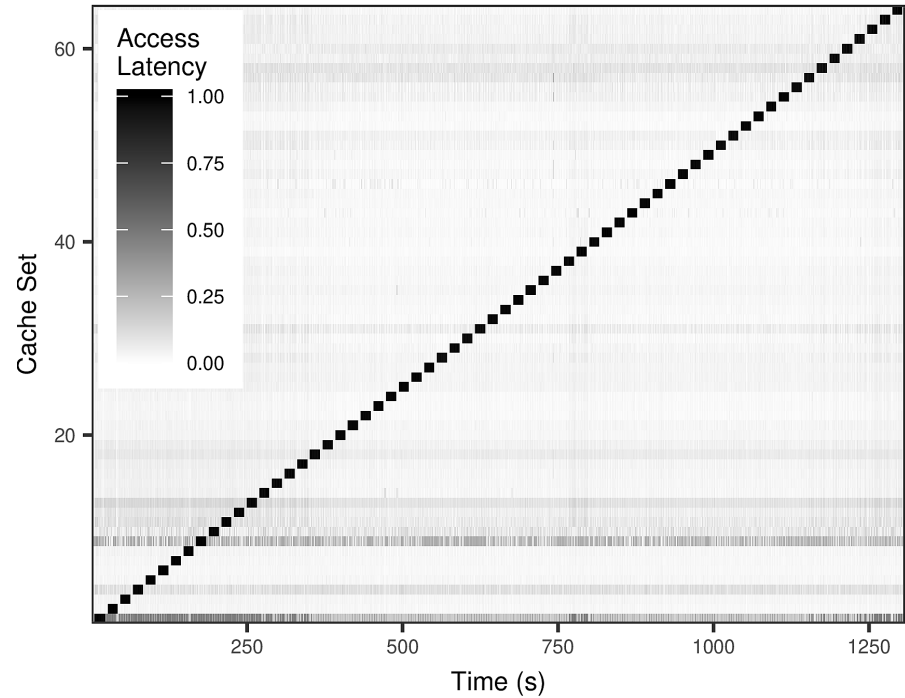
Evaluation: multithreading



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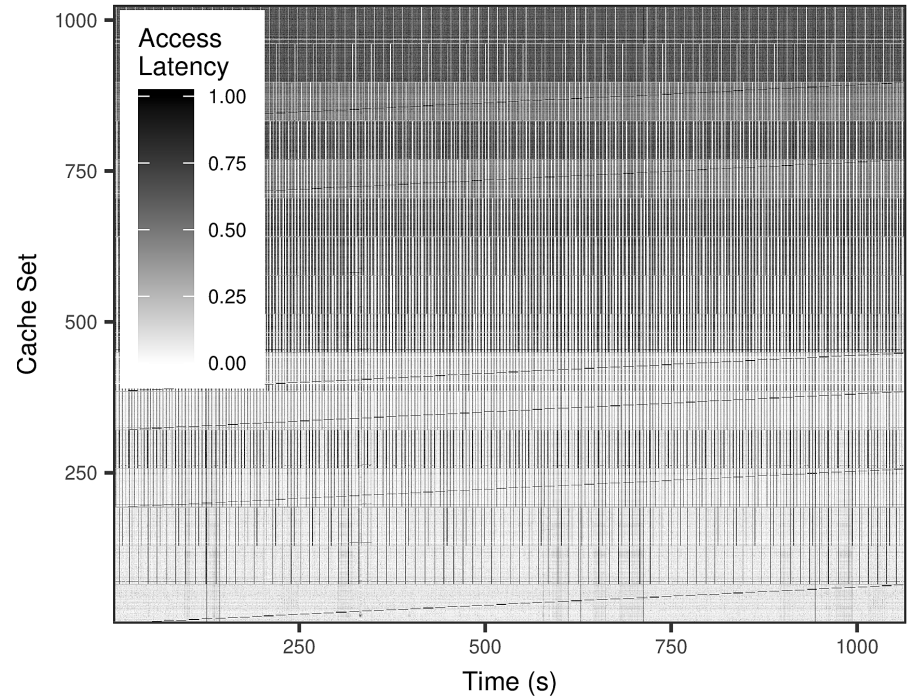
Evaluation: security

- Privileged cache SCA
 - Target: L1 cache
- No eviction



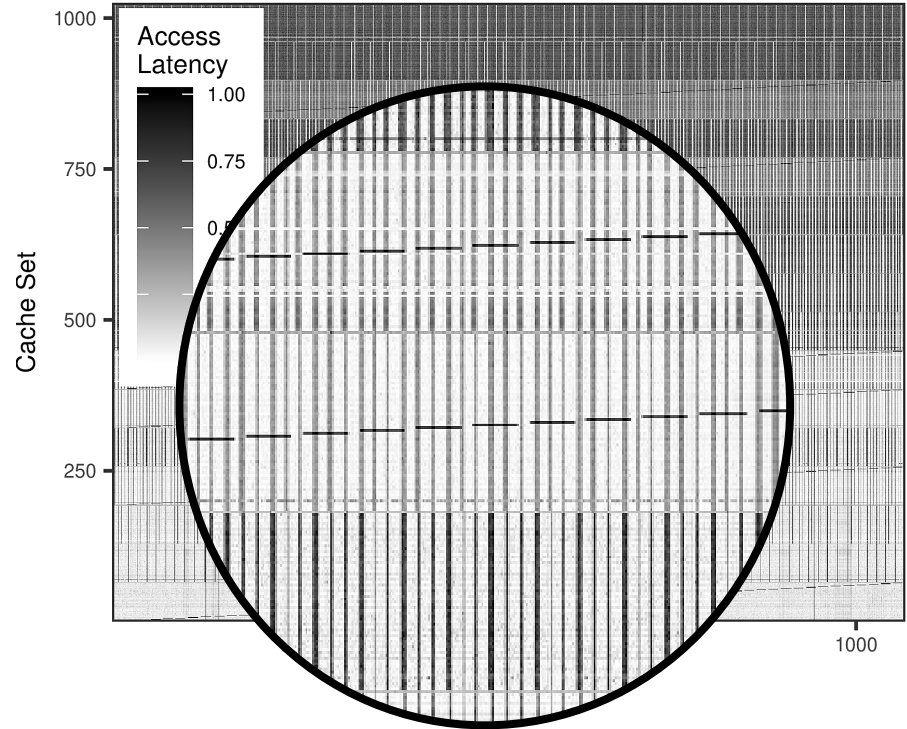
Evaluation: security

- Privileged cache SCA
 - Target: L2 cache
- No eviction



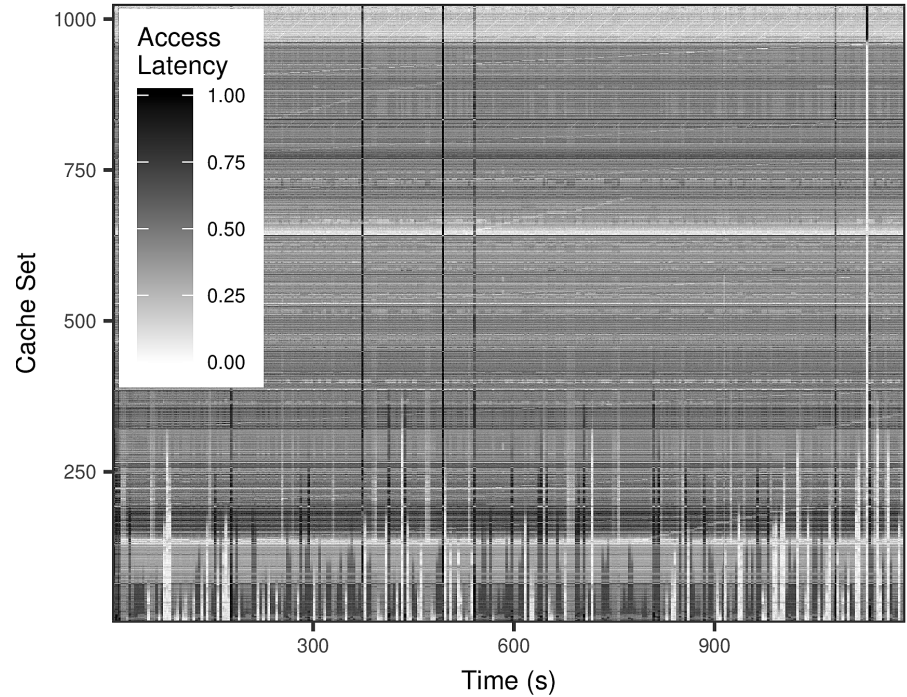
Evaluation: security

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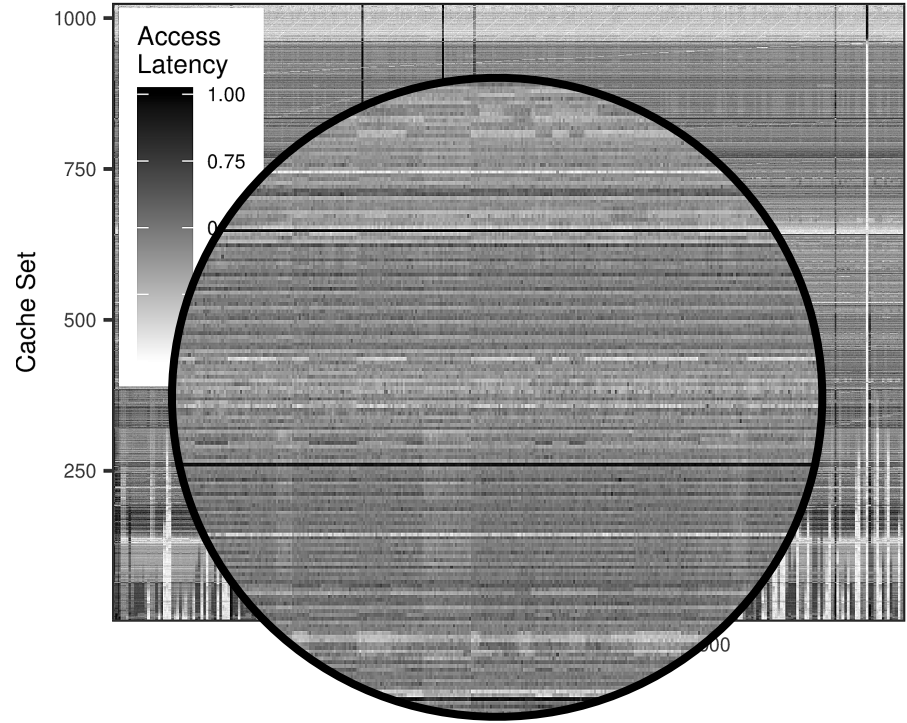
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 - Ask OS for
 - Lower interrupt rate
 - Paired thread allocation
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Thanks!

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